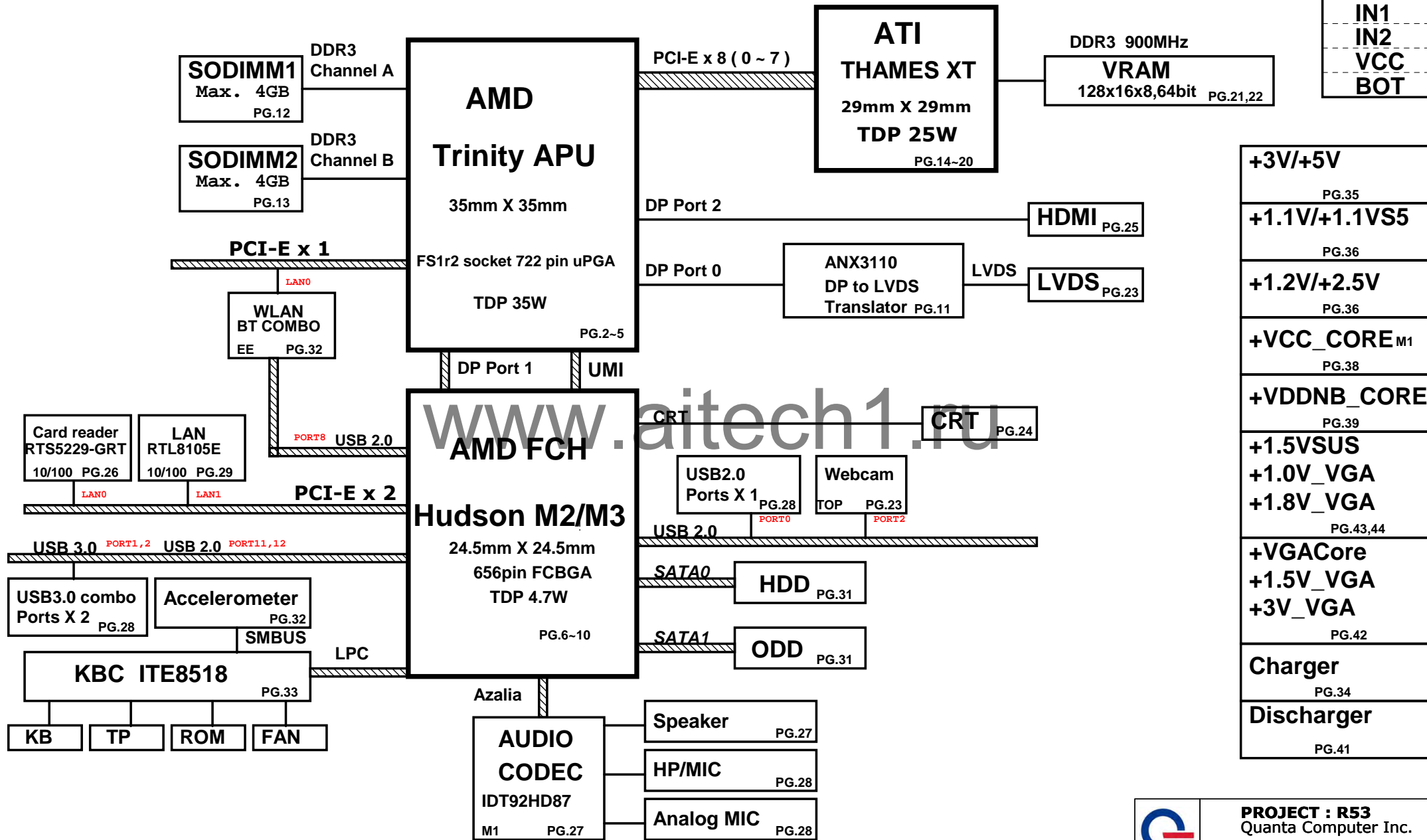
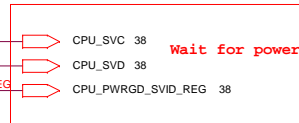


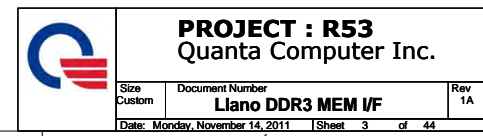
R53 AMD Comal UMA/Muxless SYSTEM DIAGRAM

Stackup

TOP
GND
IN1
IN2
VCC
BOT







DP0 output to
eDP to LVDS converter

DP1 output to Hudson-M2
for VGA translator interface

4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

note -HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Place caps with APU < 1 inch
route PCIe as 85ohm +/- 10%

Display port power 1.5V min 1.2v max : 1.65v

Display port power 1.5V min 1.2v max : 1.65v

LVDS

VGA

HDMI

To AMD HDT

Trinity APU

Thermal

APU_PROCHOT# 可以當 input or output
當Low時CPU會降P-STATE

SI, PU SUS power
meet AMD design

reserve for leakage current verify

to EC reserve only

FS#R1 signals is for detect CPU TYPE and protect it.
FS#R1 CPU this pin is N.C
FS#R2 CPU this pin is LOW
can remove it at MP

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

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4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

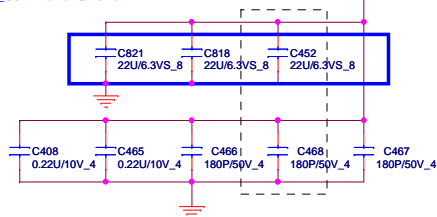
4/19 For Comal.

APU POWER TABLE

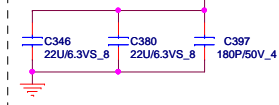
| PIN NAME | NET NAME | VOLTAGE |
|----------|-------------|---------|
| VDD | +VCC_CORE | +1.1V |
| VDDNB | +VDDNB_CORE | ?? |
| VDDIO | +1.5VSUS | +1.5V |
| VDDP | +1.2V_VDDP | +1.2V |
| VDDR | +1.2V_VDDR | +1.2V |
| VDDA | +2.5V_VDDA | +2.5V |

SI , change to 22u for improve
+VDDNB_CORE transient

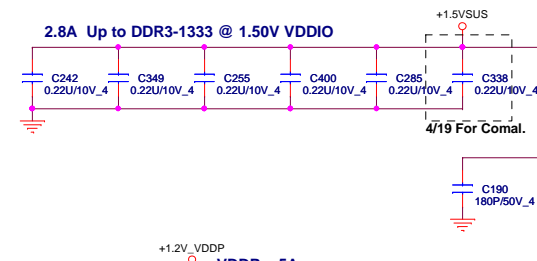
4/19 For Comal.



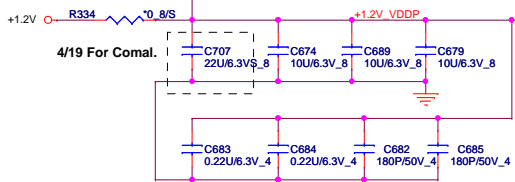
4/19 For Comal.



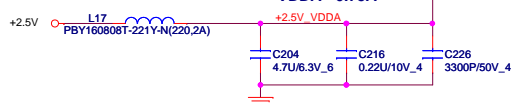
2.8A Up to DDR3-1333 @ 1.50V VDDIO



VDDP = 5A

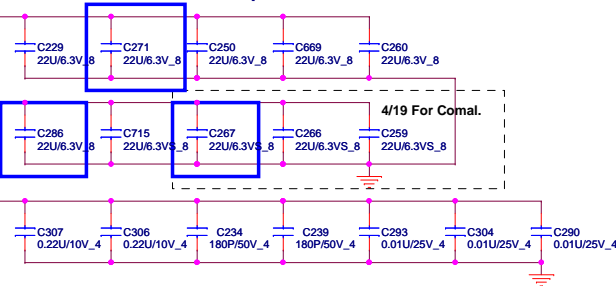


VDDA= 0.75A

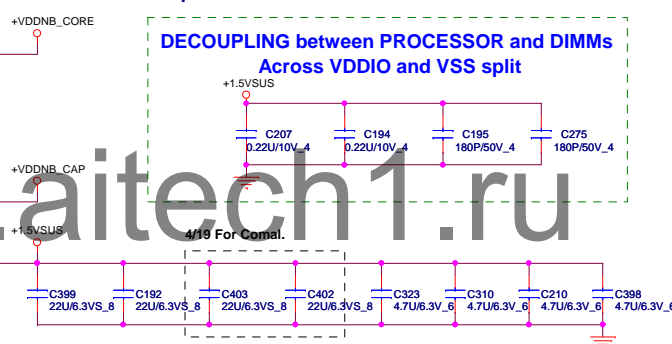


Trinity APU

36A
Maximum IDDspike 50A

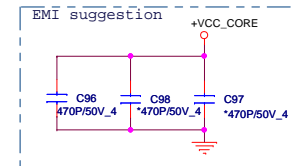
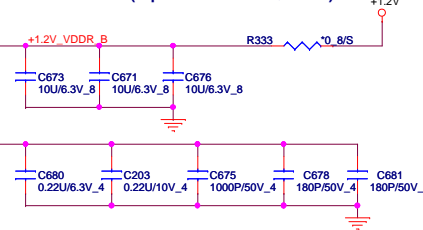


25A
Maximum IDDNBspike 33A

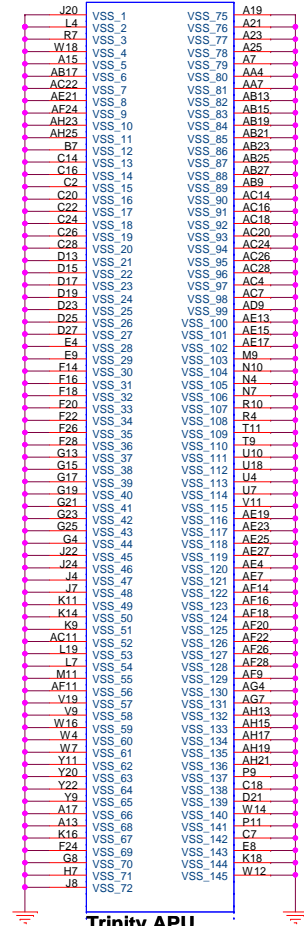


If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)



U25E



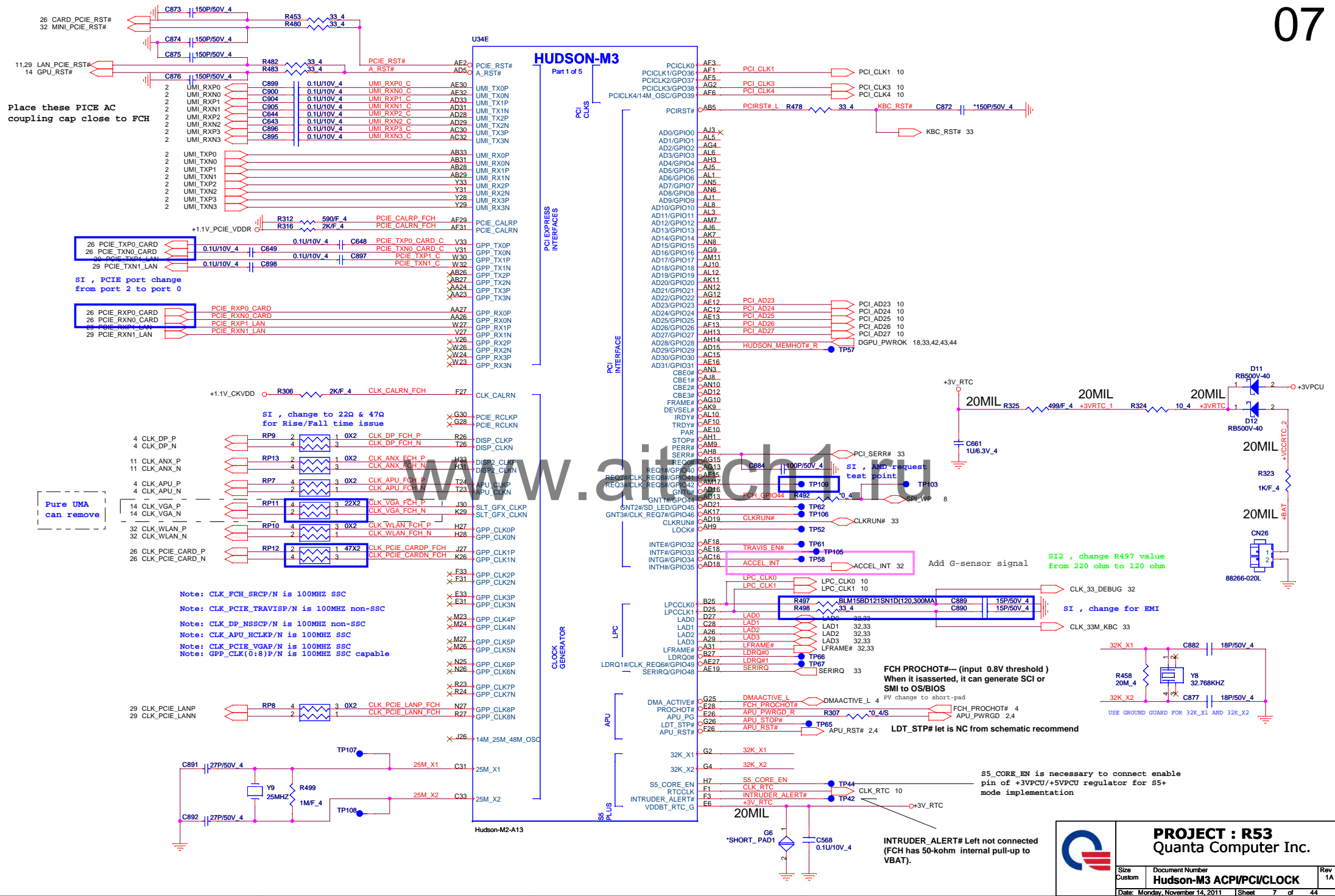
Trinity APU

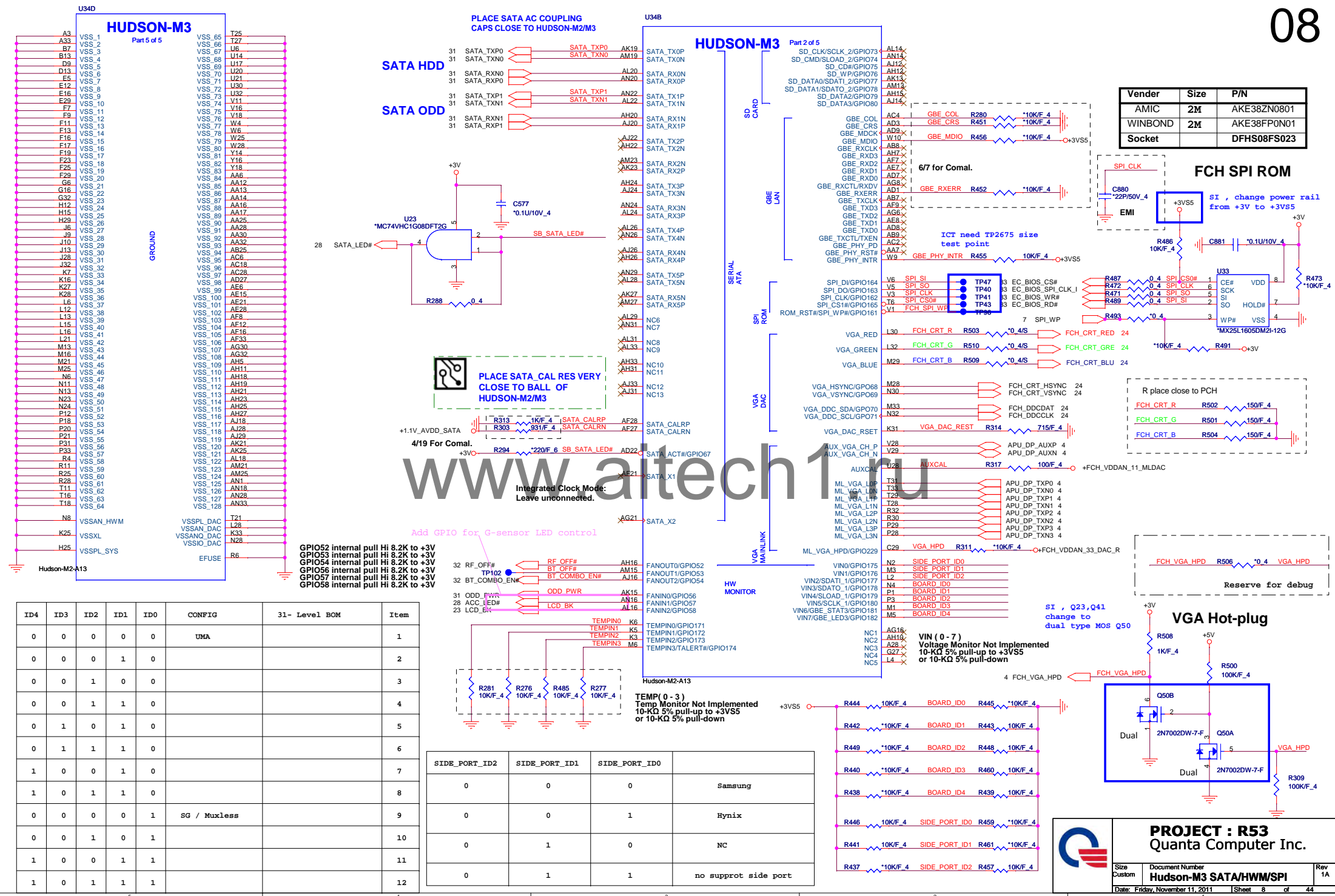


PROJECT : R53
Quanta Computer Inc.

| Size | Document Number | Rev |
|---------------------------------|-----------------|-----|
| Custom | Llano POWER/GND | 1A |
| Date: Friday, November 11, 2011 | Sheet 5 of 44 | |







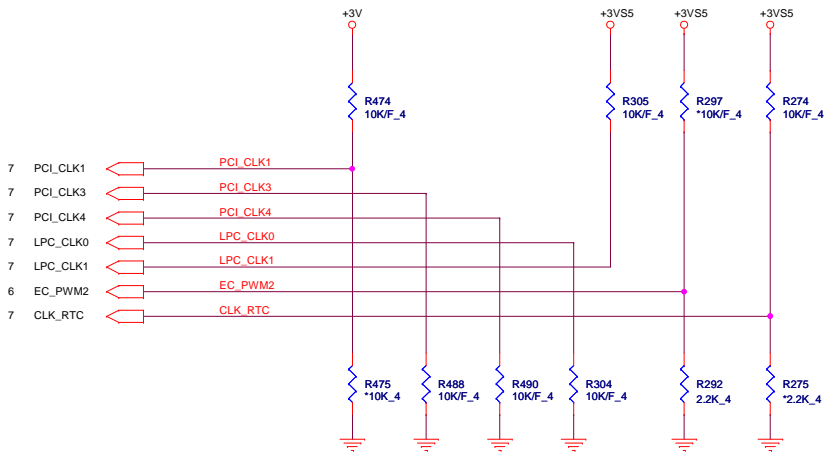
U34C



| | | |
|---------------------------------|---|---------------|
| Size Custom | Document Number Hudson-M3 POWER/GND | Rev 1A |
| Date: Friday, November 11, 2011 | | Sheet 9 of 44 |

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

| | | PCI_CLK1 | | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | EC_PWM2 | CLK_RTC |
|-----------|-------|-----------------------------------|-------|-------------------------------------|---------------------------------|----------------------------|----------------------------------|--------------------------------|-------------------------------------|
| PULL HIGH | ----- | ALLOW PCIE Gen2 DEFAULT | ----- | USE DEBUG STRAP | non Fusion CLOCK MODE | AMD internal EC ENABLED | CLKGEN ENABLED DEFAULT | LPC ROM DEFAULT | S5 PLUS MODE ENABLED |
| PULL LOW | ----- | FORCE PCIE Gen1 | ----- | IGNORE DEBUG STRAP DEFAULT | FUSION CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLED | SPI ROM DISABLED DEFAULT | S5 PLUS MODE DISABLED DEFAULT |

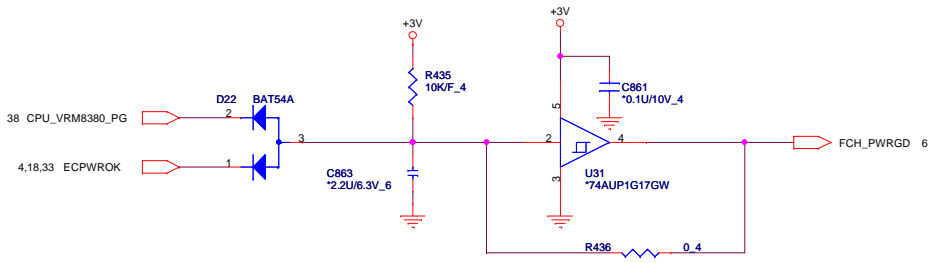
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

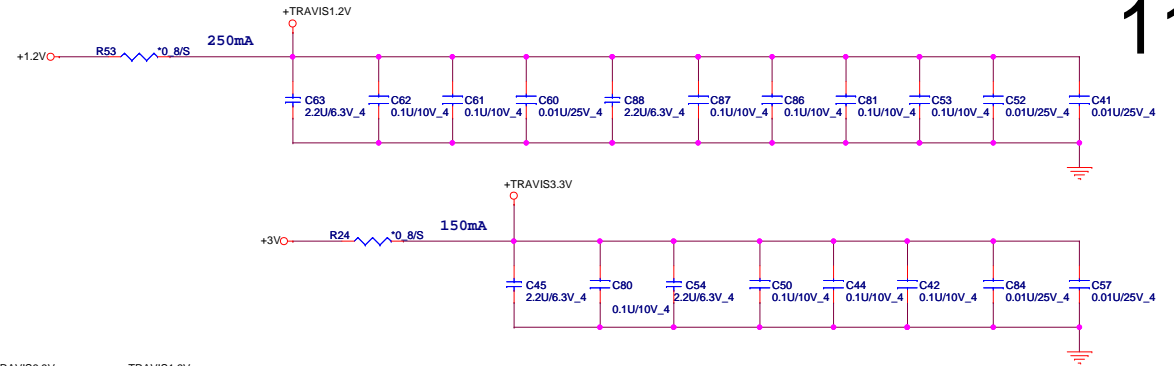
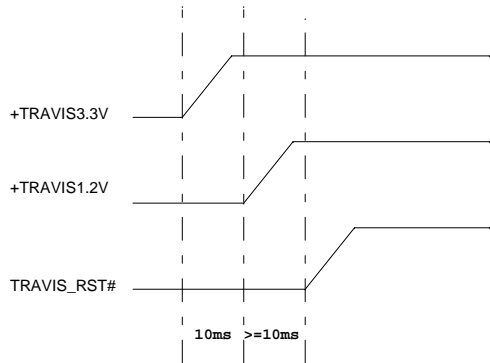


| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|-----------|-------------------------------|---------------------------------------|------------------------------|---|--|
| PULL HIGH | USE PCI PLL DEFAULT | DISABLE ILA AUTORUN DEFAULT | USE FC PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |

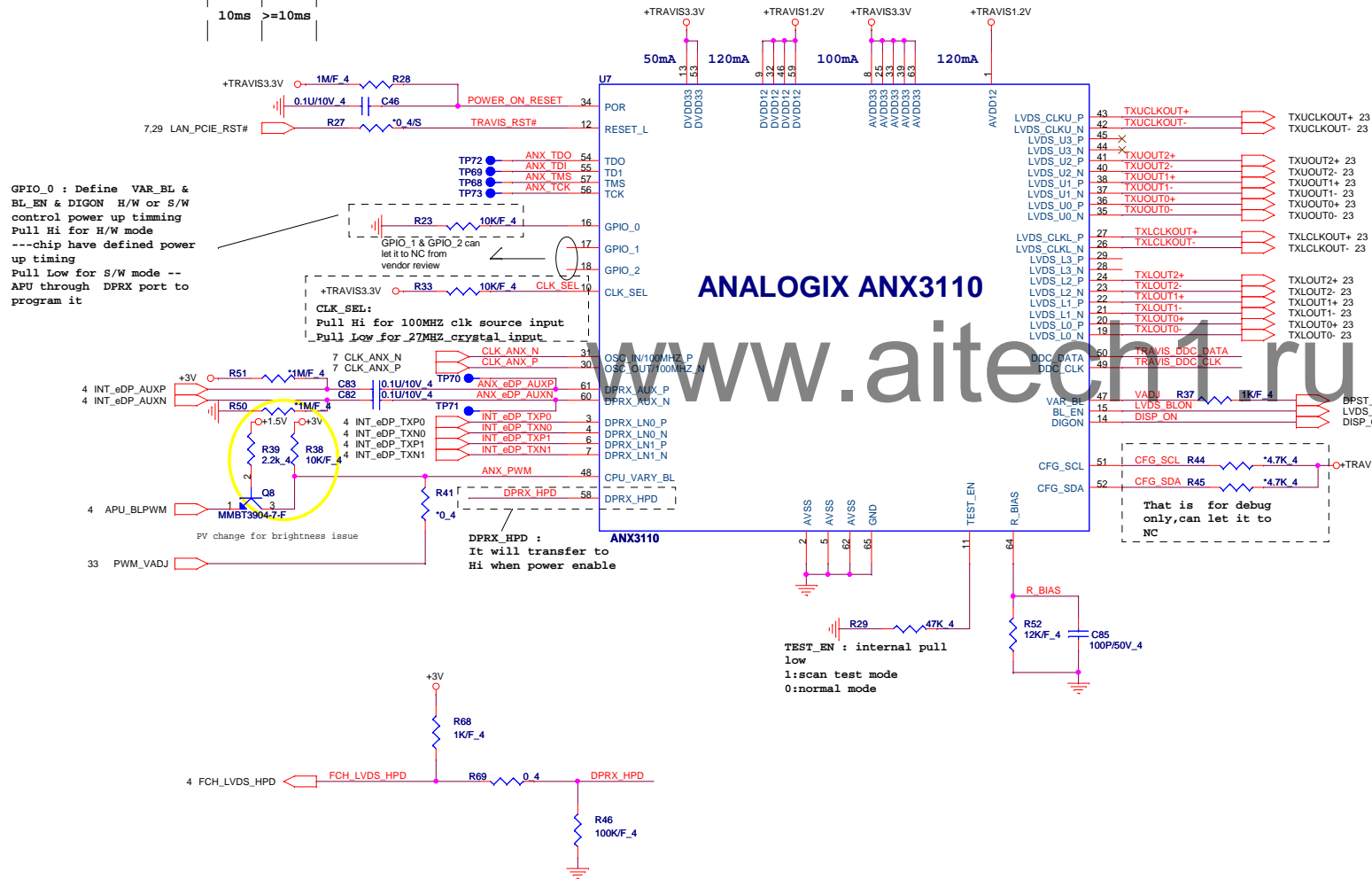
FCH_PWRGD



ANX3110 Power Up Sequence

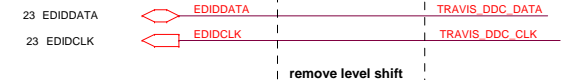


GPIO_0 : Define VAR_BL & BL_EN & DIGON H/W or S/W control power up timing Pull Hi for H/W mode ---chip have defined power up timing Pull Low for S/W mode -- APU through DPRX port to program it




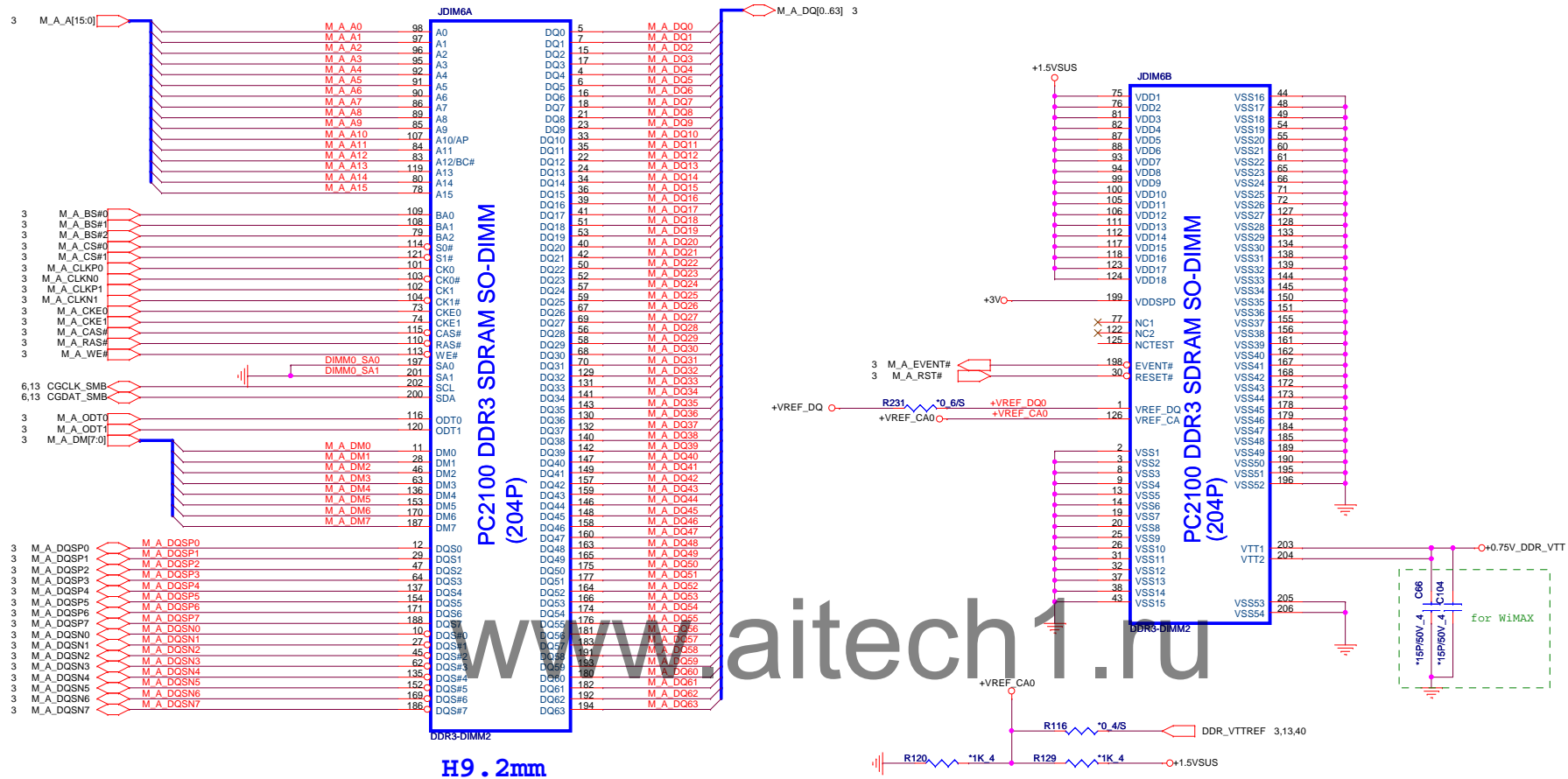
ANALOGIX ANX3110

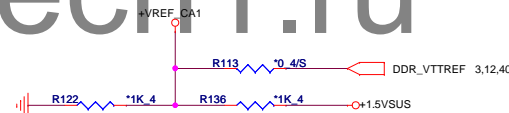
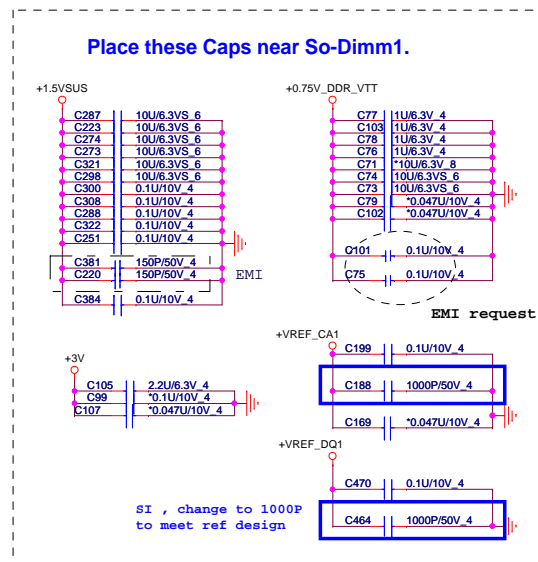
www.aitech1.ru



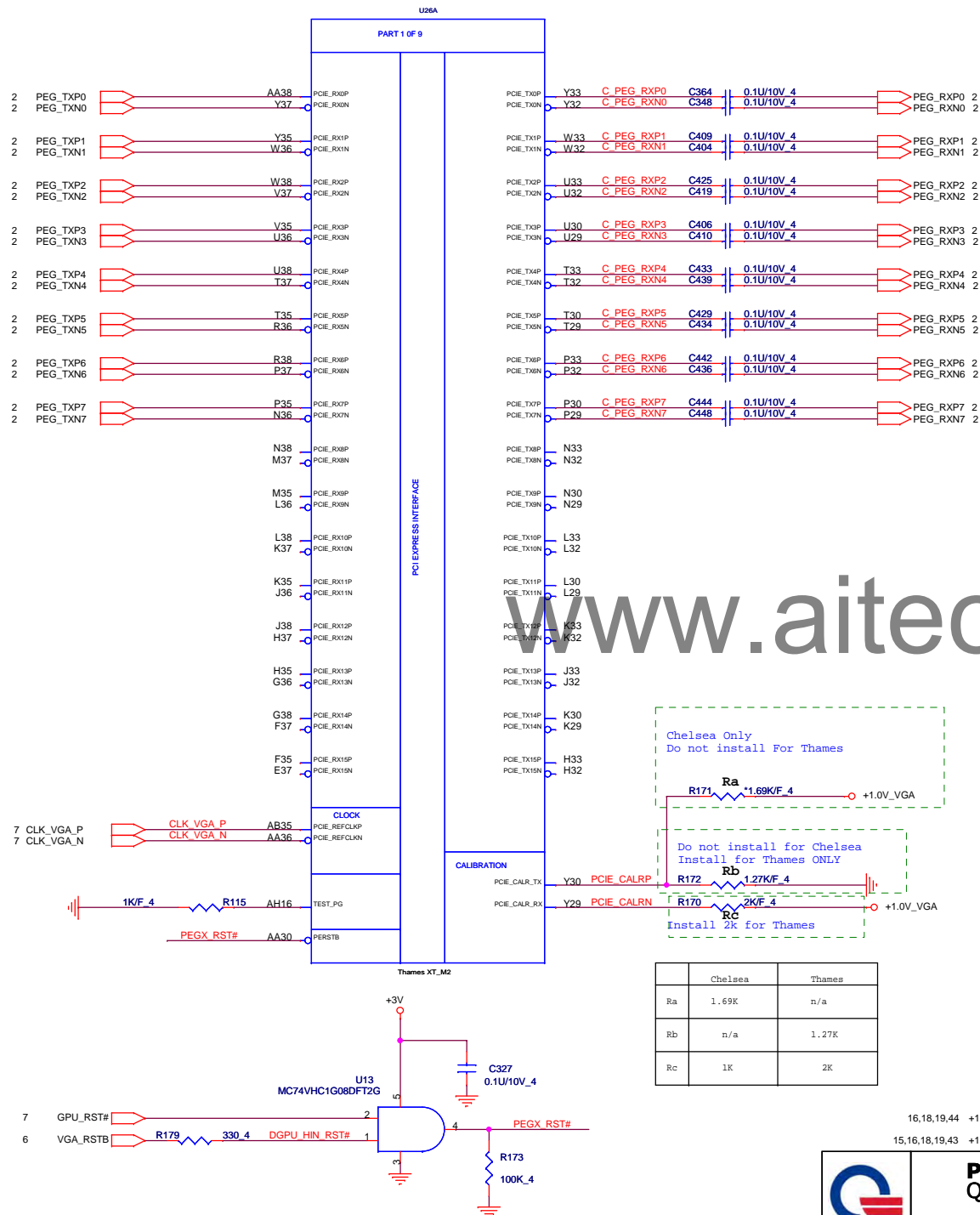
That is for debug only, can let it to NC

| | | | | |
|---|-----------------|-------|--|--|
|  | | | PROJECT : R53 Quanta Computer Inc. | |
| Size Custom | Document Number | | Rev 1A | |
| | ANX3110 | | | |
| Date: Friday, November 11, 2011 | Sheet 11 | of 44 | | |



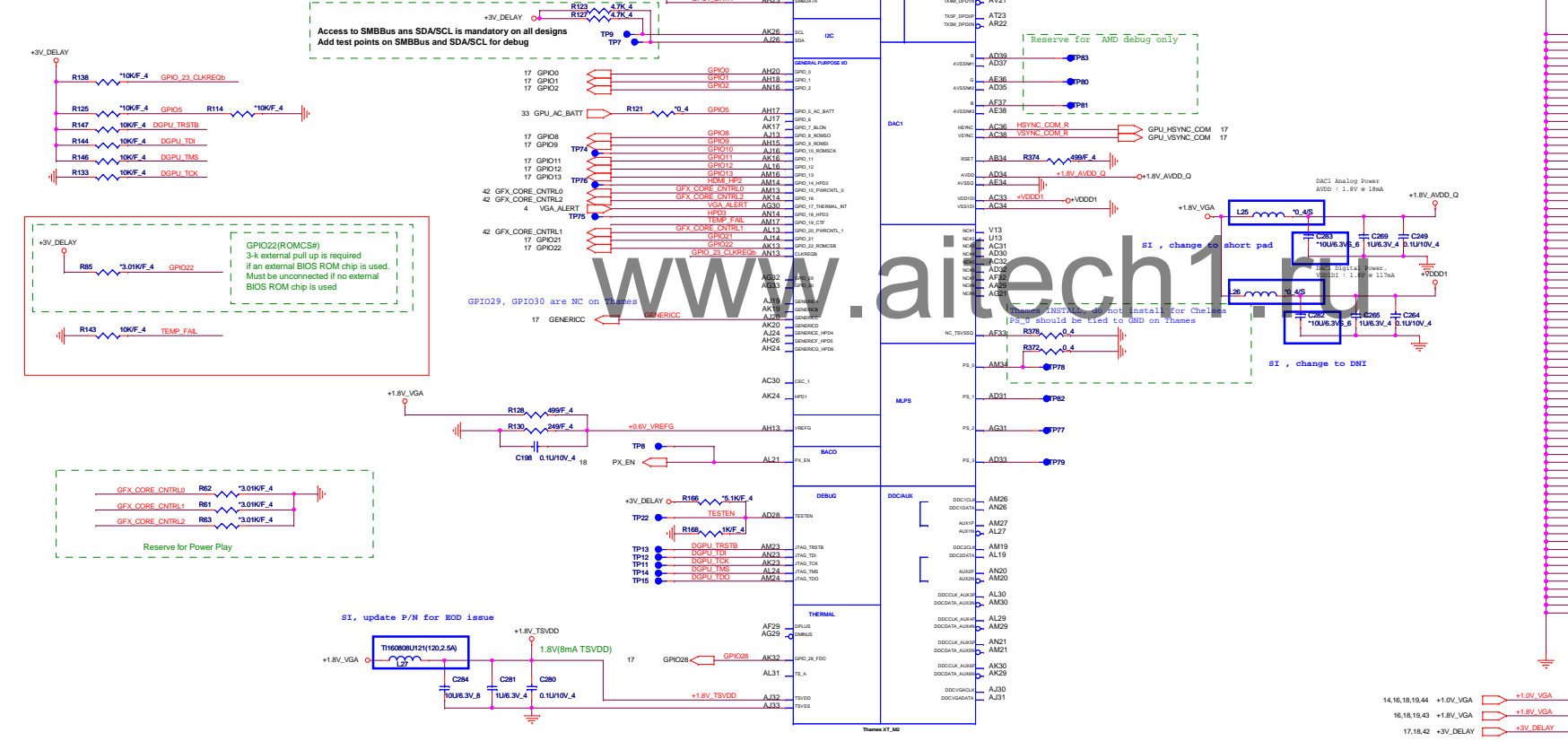


12,40 +0.75V_DDR_VTT
4,5,12,40,41,44 +1.5VSUS
0,31,32,33,41,42,44 +3V

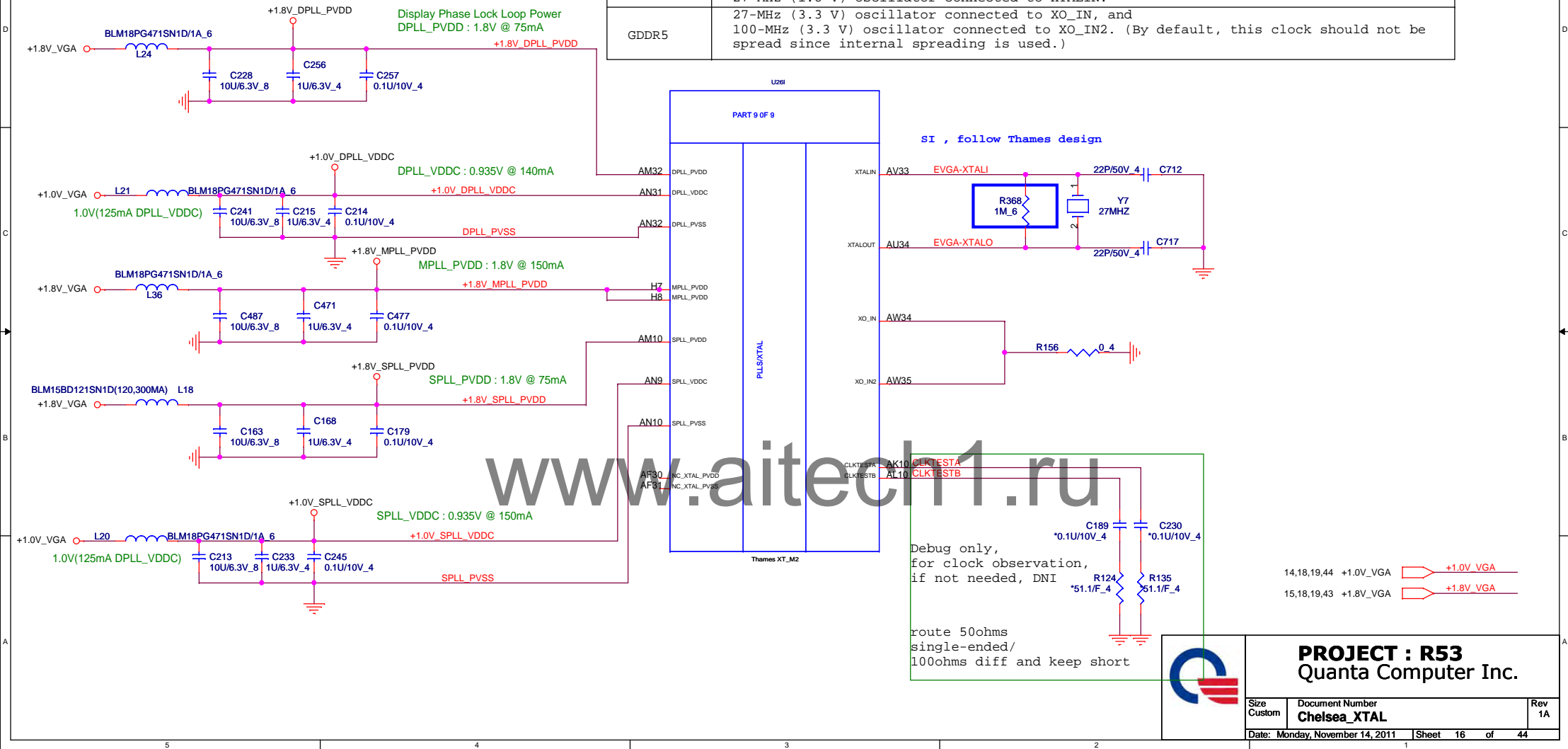


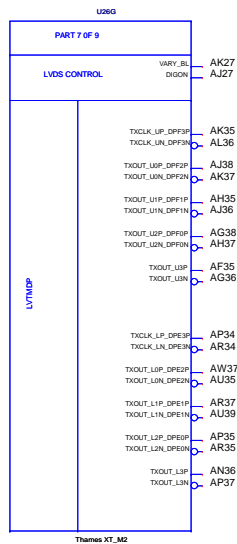
PROJECT : R53
Quanta Computer Inc.

| | GPI016 | GPI020 | GPI015 | |
|-----------|----------|----------|----------|----------|
| Thanes-XT | PWRNTL 2 | PWRNTL 1 | PWRNTL 0 | VGA CORE |
| L | 0 | 0 | 0 | 1.0V |
| M | 0 | 0 | 1 | 0.9V |
| H | 0 | 1 | 0 | 0.875V |
| | 0 | 1 | 1 | 0.85V |
| | 1 | 0 | 0 | 0.8V |
| | 1 | 0 | 1 | 0.75V |



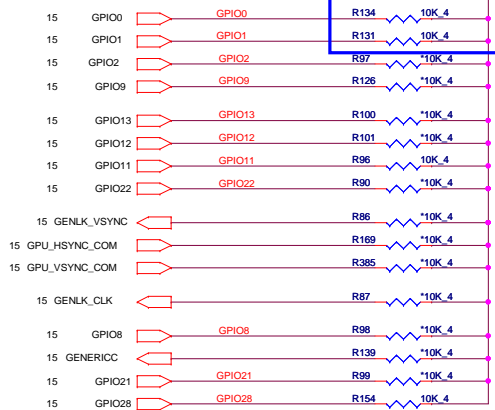
| Memory Type | |
|-------------|---|
| DDR3 | 27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN. |
| GDDR5 | 27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.) |





SI , default setting should be PU
from AMD SCH review result

+3V_DELAY



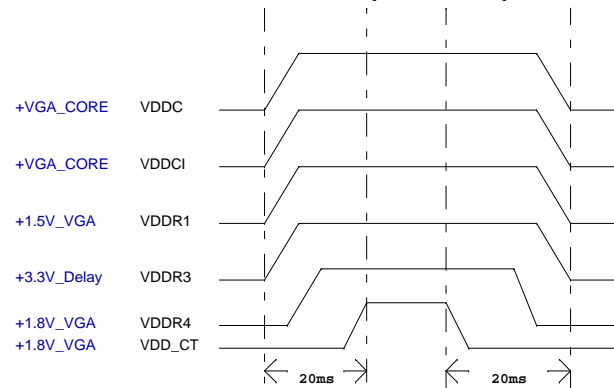
Memory Aperture size

| GPIO9 BIOSROM | | GPIO13 ROMIDCFG2 | GPIO12 ROMIDCFG1 | GPIO11 ROMIDCFG0 |
|------------------|------|---------------------|---------------------|---------------------|
| 0 | 128M | 0 | 0 | 0 |
| 0 | 256M | 0 | 0 | 1 |
| 0 | 64M | 0 | 1 | 0 |
| 0 | 32M | 0 | 1 | 1 |
| 0 | 512M | 1 | 0 | 0 |
| 0 | 1G | 1 | 0 | 1 |
| 0 | 2G | 1 | 1 | 0 |
| 0 | 4G | 1 | 1 | 1 |

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

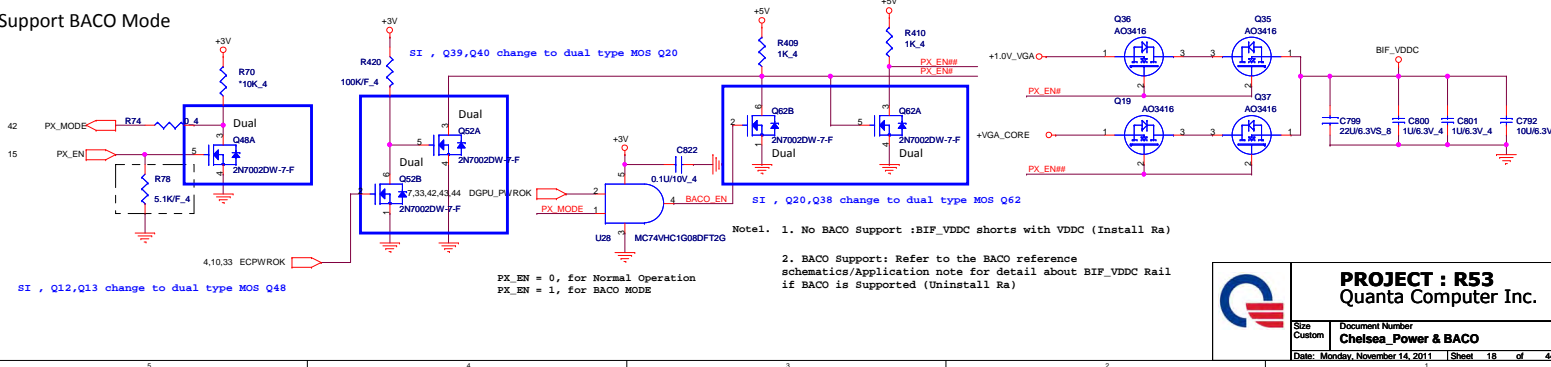
| CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET | | | | |
|---|--------------------------------|--|---|------------------|
| STRAPS | MLPS | GPIO PIN | DESCRIPTION OF DEFAULT SETTINGS | Default Setting |
| MLPS_DISABLE | NA | GPIO_28_FDO | Enable MLPS. NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP | X |
| TX_PWRS_ENB | PS_1[4] | GPIO0 | Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing | X |
| TX_DEEMPH_EN | PS_1[5] | GPIO1 | PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled | X |
| BIF_GEN3_EN_A | PS_1[1] | GPIO2 | PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on | 1 |
| BIF_VGA DIS | PS_2[4] | GPIO9 | VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU) | 0 |
| ROMIDCFG[2:0] | PS_0[3..1] | GPIO[13:11] | Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 2Mbit M25P10A (ST) 101 - 4Mbit M25P40 (ST) 100 - 512Kbit M25LV512 (Chingis) 101 - 1Mbit M25LV010 (Chingis) | XXX |
| BIOS_ROM_EN | PS_2[3] | GPIO22 | Enable external BIOS ROM device 0: Disabled 1: Enabled | X |
| AUD[1] AUD[0] | NA NA | HSYNC VSYNC | 00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature. | XX |
| CEC_DIS | PS_0[4] | GENLK_VSYNC | Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled | X |
| RESERVED RESERVED RESERVED RESERVED | PS_1[3] PS_1[2] NA NA | GENLK_CLK GPIO8 GPIO21 GENERICC | Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only) | 0 0 0 0 |
| AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0] | PS_3[5] PS_3[4] PS_0[5] | NA NA NA | STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable | XXX |

Power Up/Down Sequence



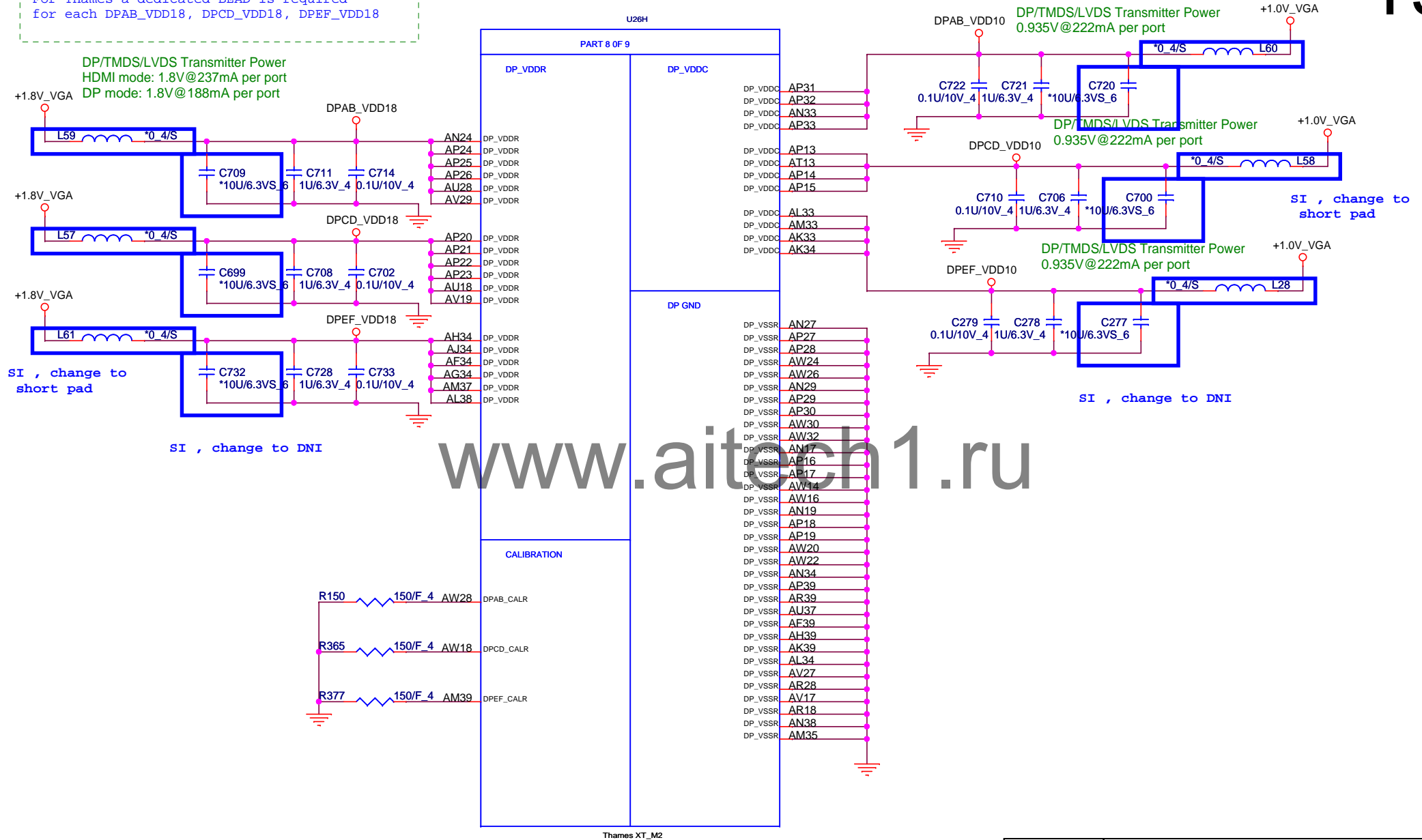
PROJECT : R53
Quanta Computer Inc.

| | | |
|---------------------------------|--|-----------|
| Size Custom | Document Number Chelsea_LVDS / STRAP | Rev 1A |
| Date: Friday, November 11, 2011 | Sheet 17 of 44 | |



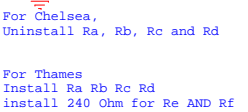
For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

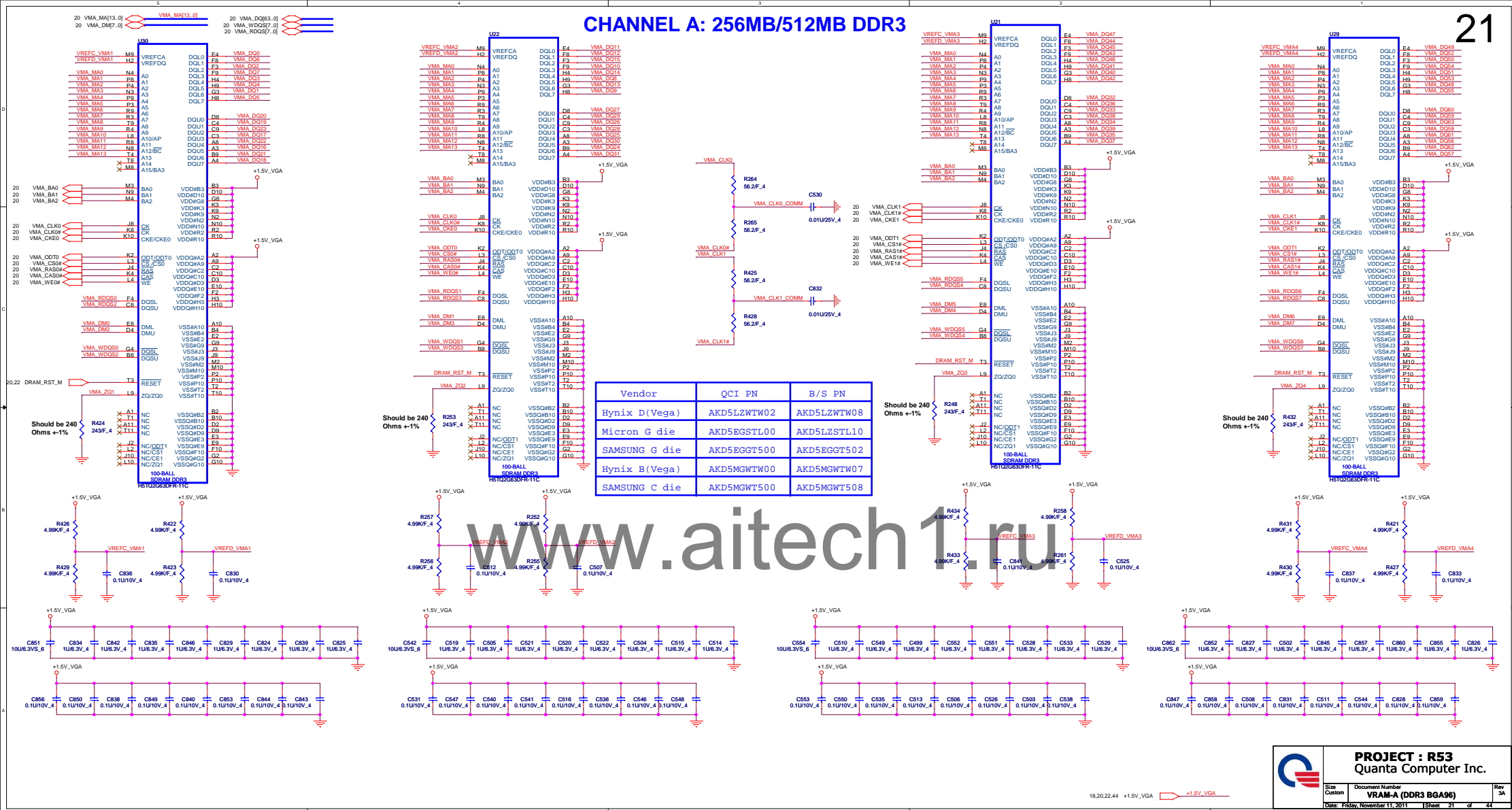


PROJECT : R53
Quanta Computer Inc.

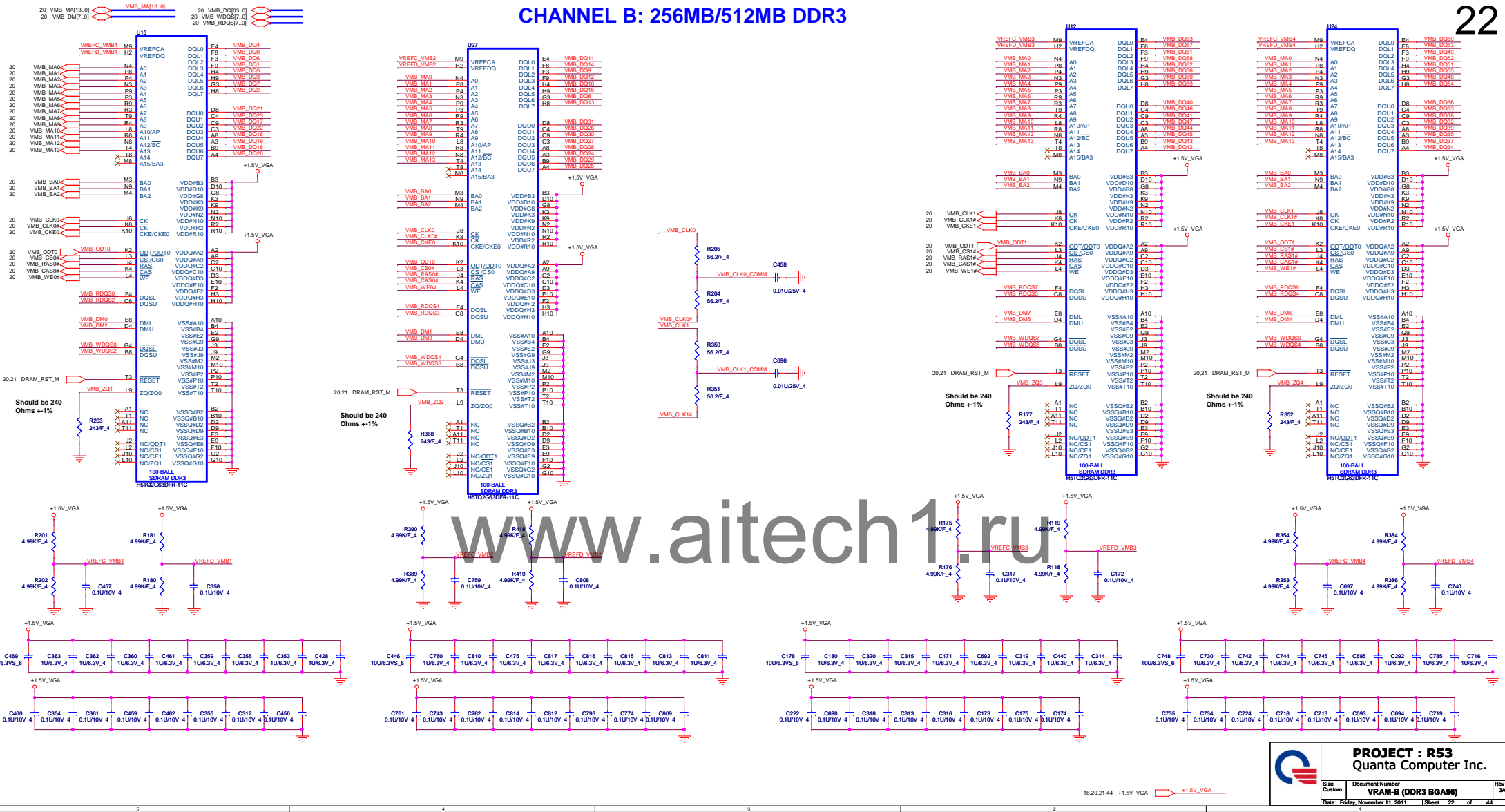
| | | |
|---------------------------------|---|-----------|
| Size Custom | Document Number Chelsea_DP Powers | Rev 1A |
| Date: Monday, November 14, 2011 | Sheet 19 of 44 | |

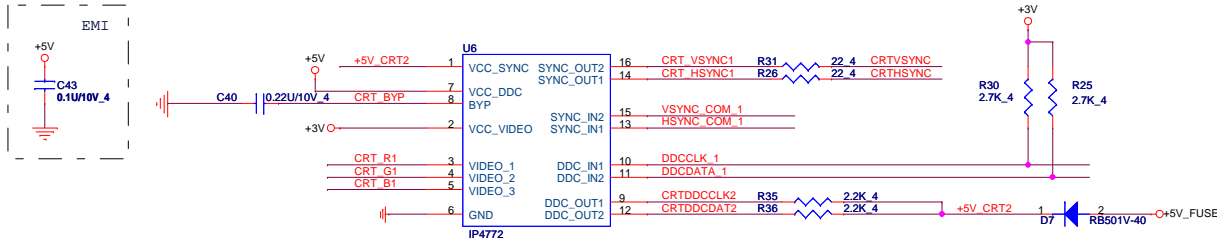
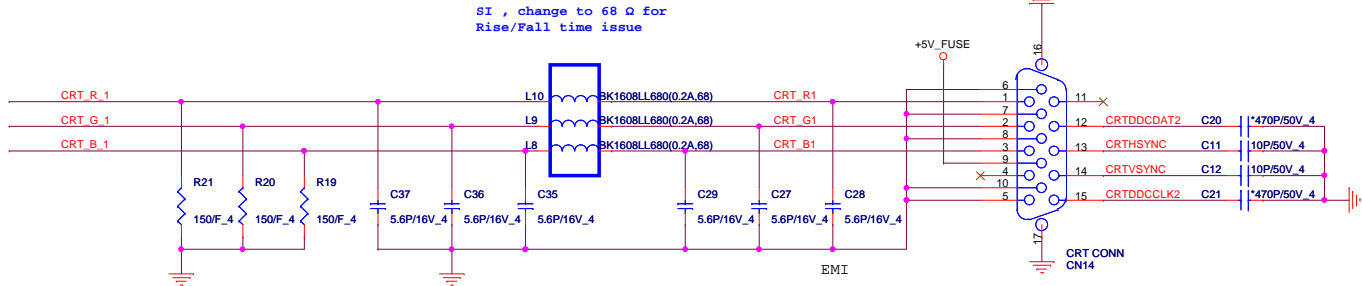
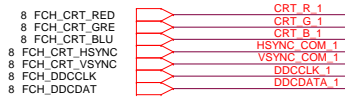


CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3

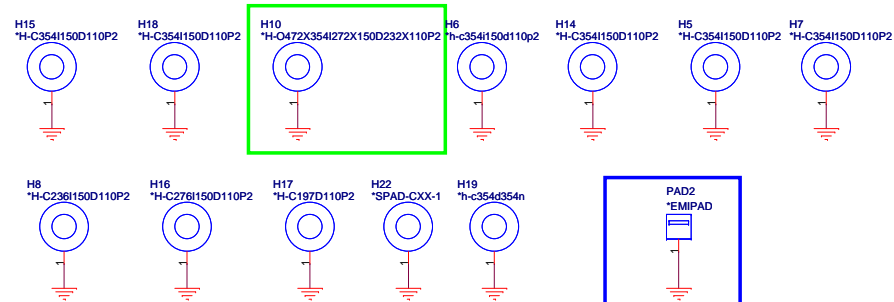




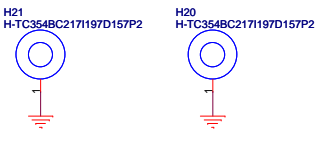
www.aitech1.ru

HOLE

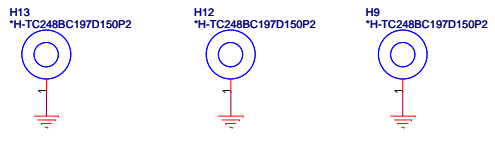
SI2, update footprint



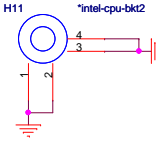
FCH NUT

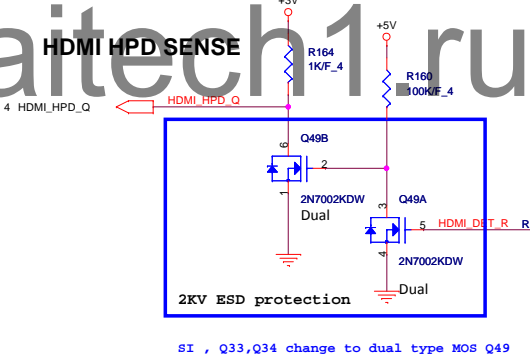
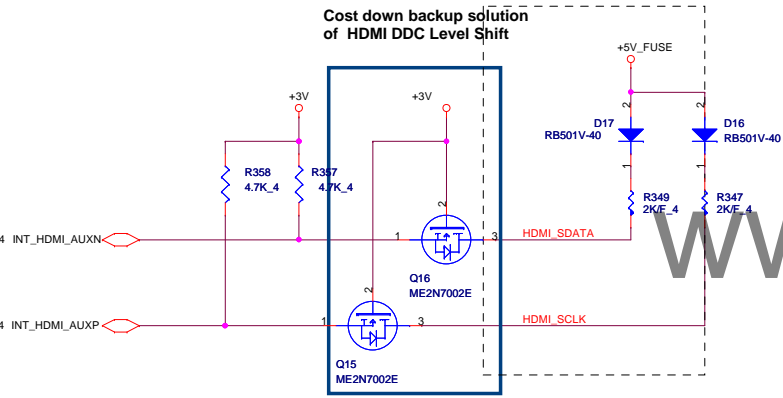
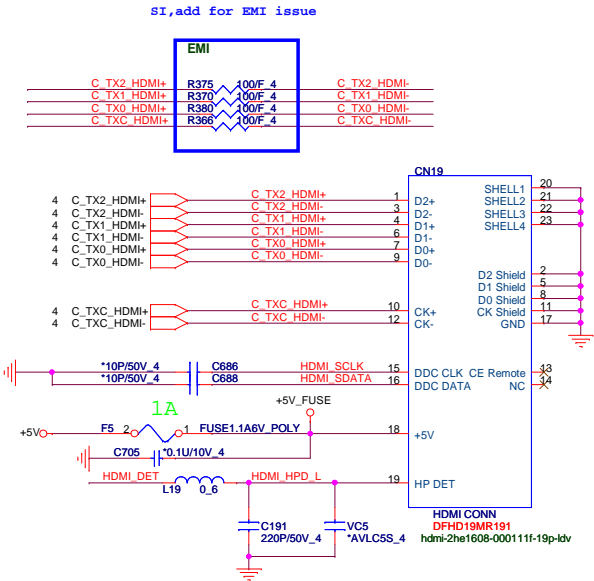
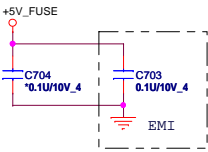
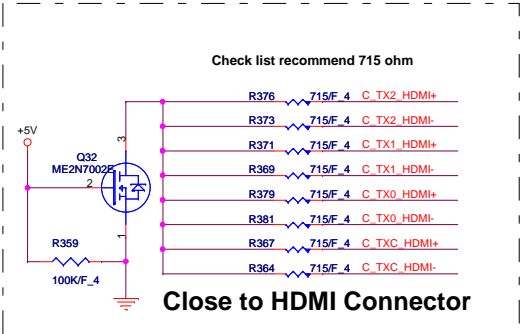


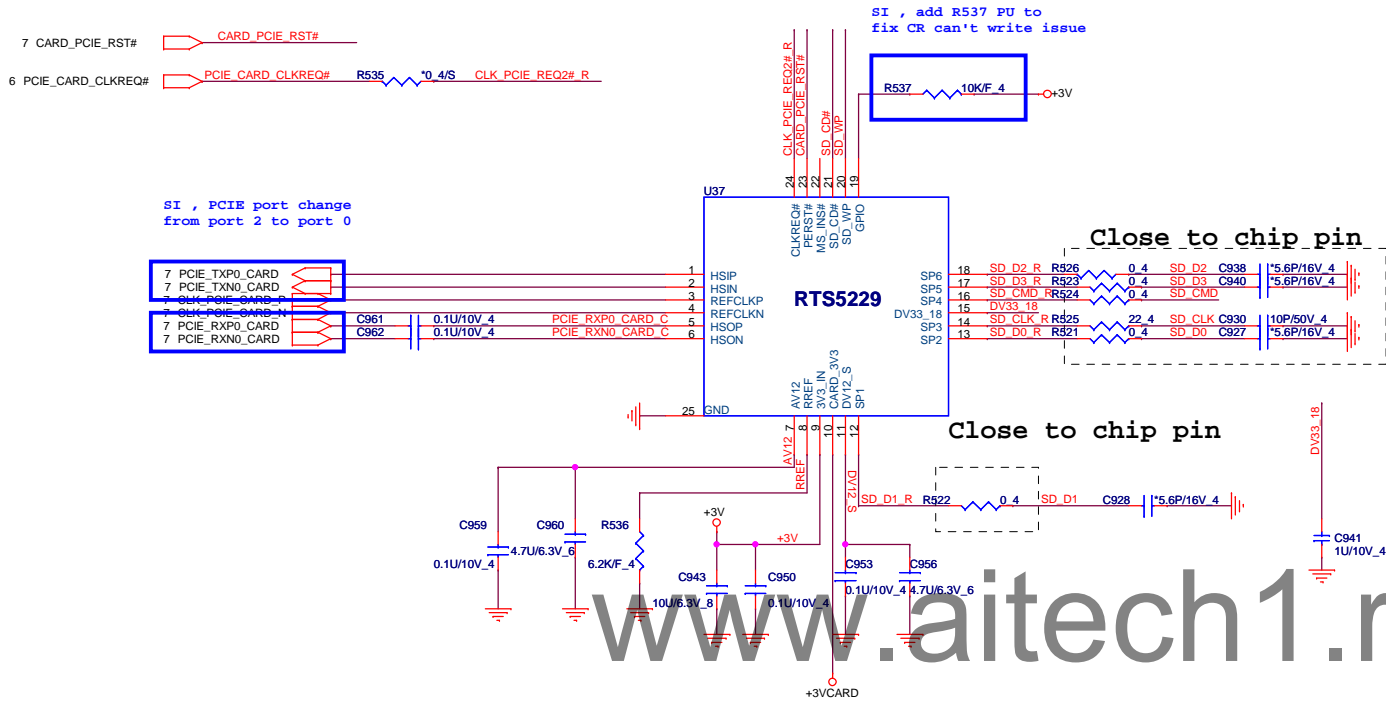
VGA BKT



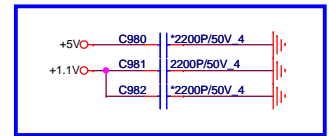
APU BKT





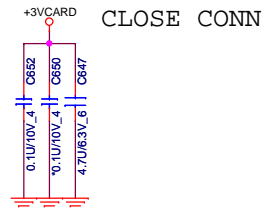
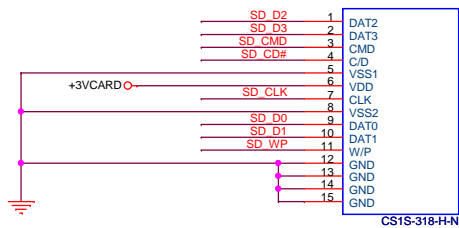


SI , EMI reserve for debug



SI, add C981 for EMI issue

SD / MMC CARD READER CN12



PROJECT : R53
Quanta Computer Inc.

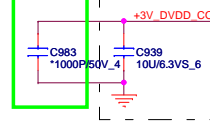
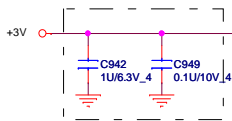
| Size | Document Number | Rev |
|---------------------------------|----------------------------|-----|
| Custom | RTS5219 & CR SOCKET & HOLE | 1A |
| Date: Monday, November 14, 2011 | Sheet 26 of 44 | |

2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,28,29,30,31,32,33,41,42,44

8,18,24,25,26,30,31,32,41

Close to CODEC

Close to CODEC

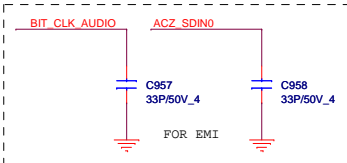
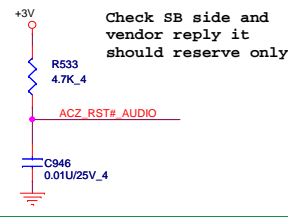
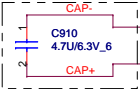


HDA Bus

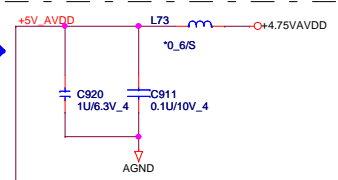
TO Digital MIC



Close to CODEC

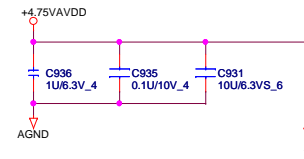


>40mils trace

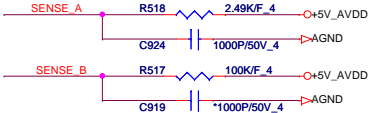


Close to CODEC

>40mils trace



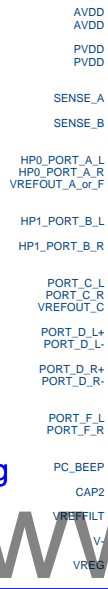
Vset=1.242V



Close to CODEC

TO Headphone jack

Digital

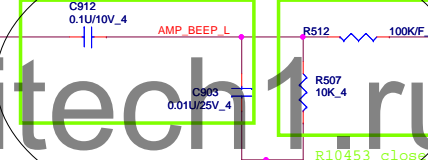


Analog

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TO Internal Speakers

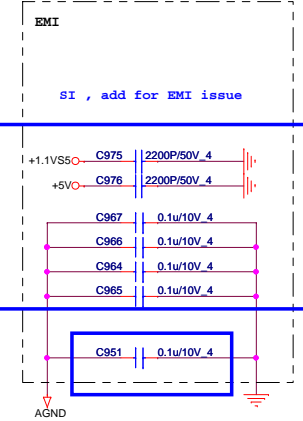
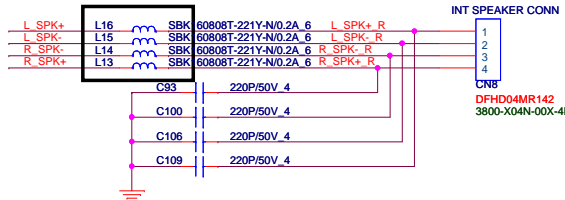
C10625 close C10629, and C10625 close Chip



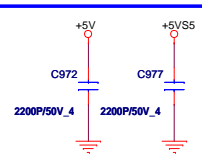
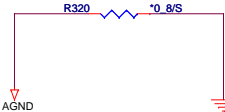
Check layout mount location

EMI Request

INT. SPEAKER



SI, EMI change to 0.1u

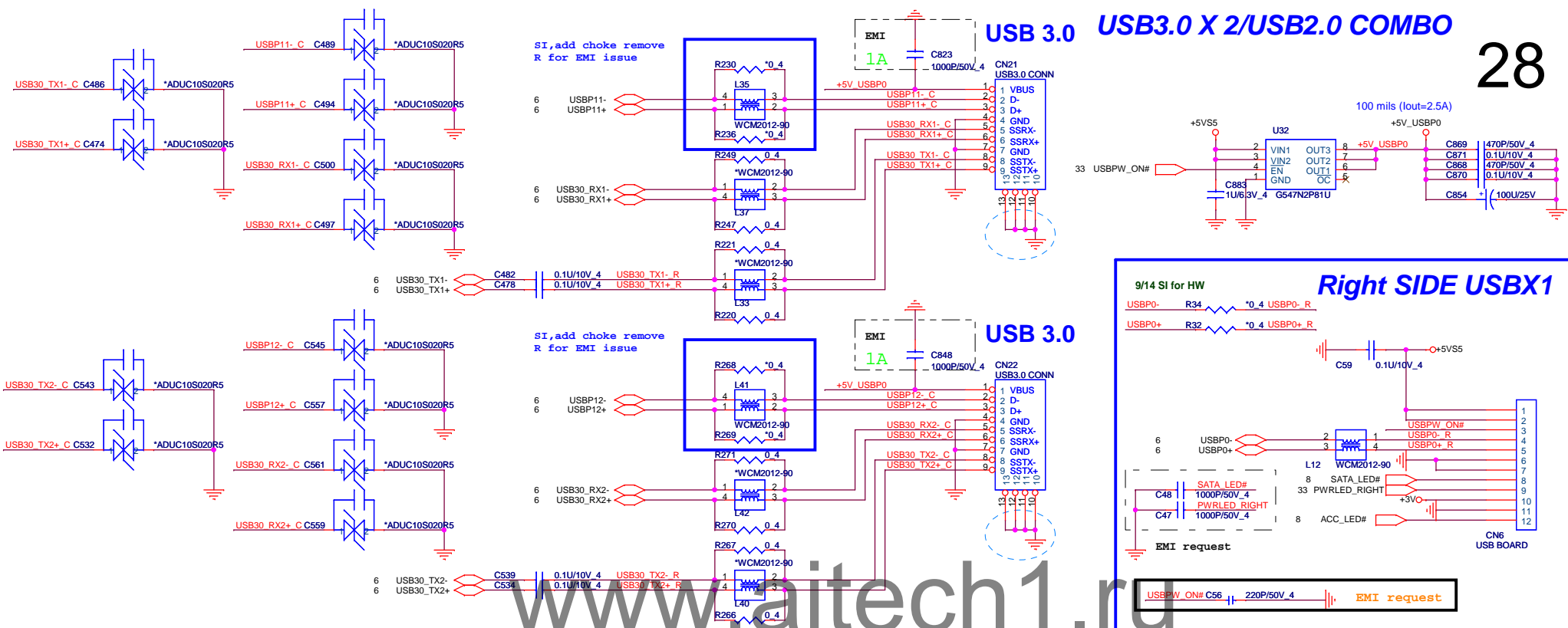


SI, add for EMI debug

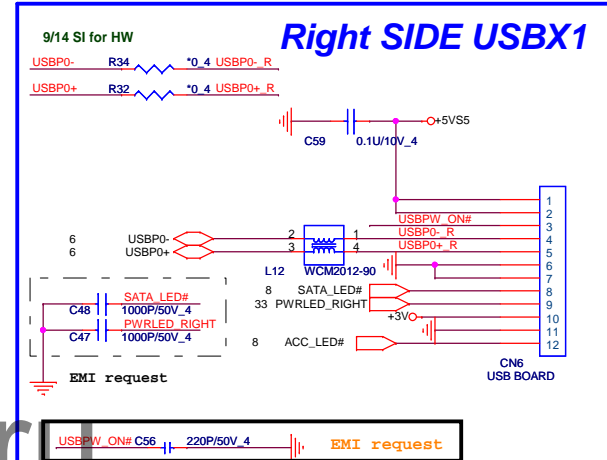
PROJECT : R53
Quanta Computer Inc.

| Size | Document Number | Rev |
|---------------------------------|-----------------|-----|
| Custom | Azalia 92HD80 | 1A |
| Date: Friday, November 11, 2011 | Sheet 27 of 44 | |

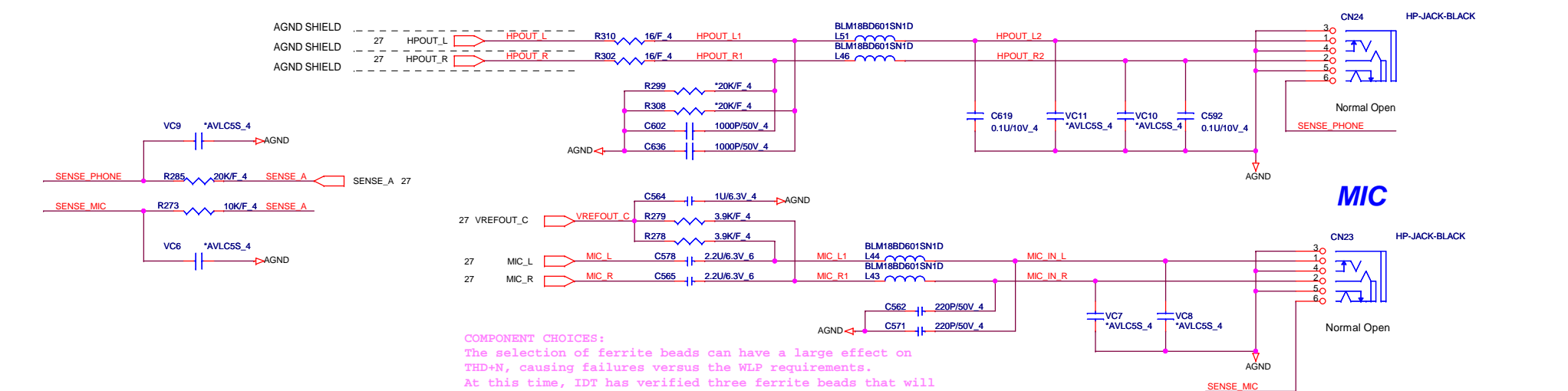
USB 3.0 USB3.0 X 2/USB2.0 COMBO



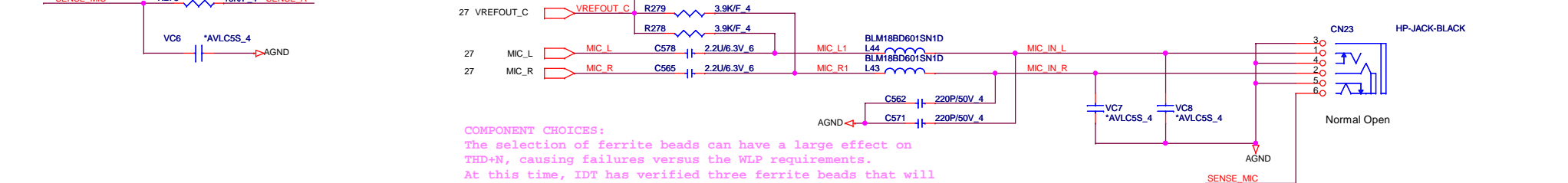
Right SIDE USBX1



Line out



MIC



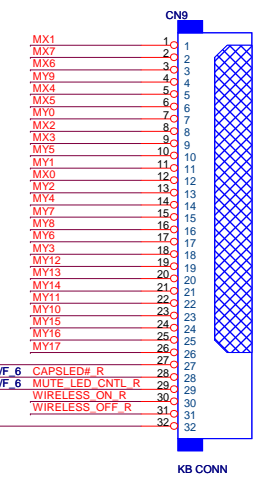
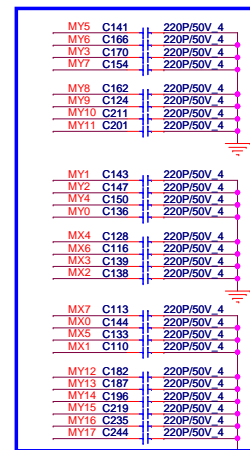
COMPONENT CHOICES:
 The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements. At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
 Murata: BLM18BD601SN1
 TDK: MMZ1608Y601BTA
 Taiyo Yuden: LF BK 1608HM601-T

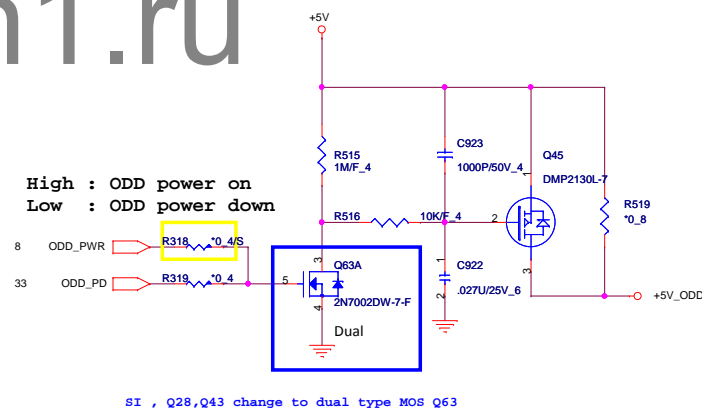
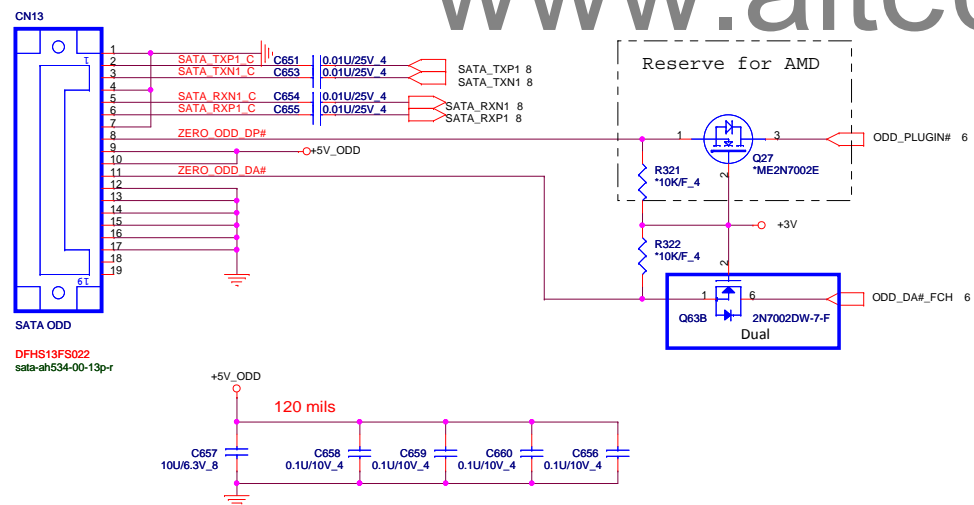
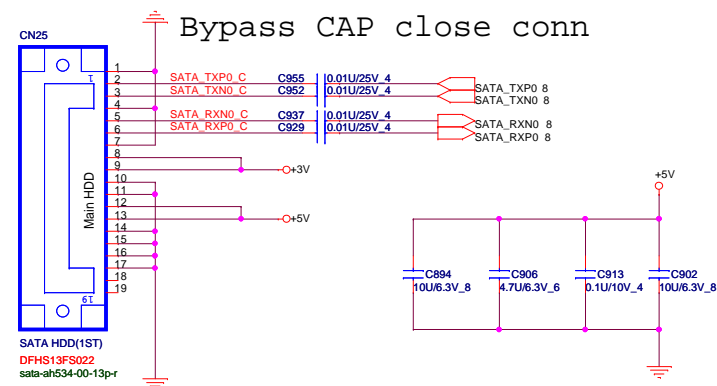


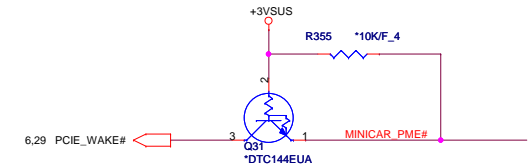
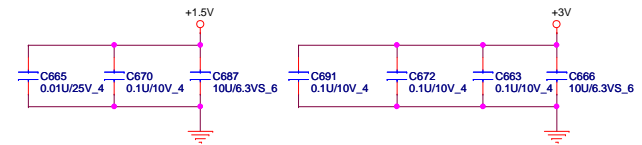
PROJECT : R53
 Quanta Computer Inc.

| Size | Document Number | Rev |
|--------|---------------------------|----------------|
| Custom | USB/BT/Audio Jack | 1A |
| Date: | Monday, November 14, 2011 | Sheet 28 of 44 |

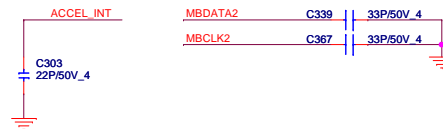
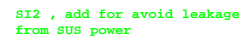
KEYBOARD Con.

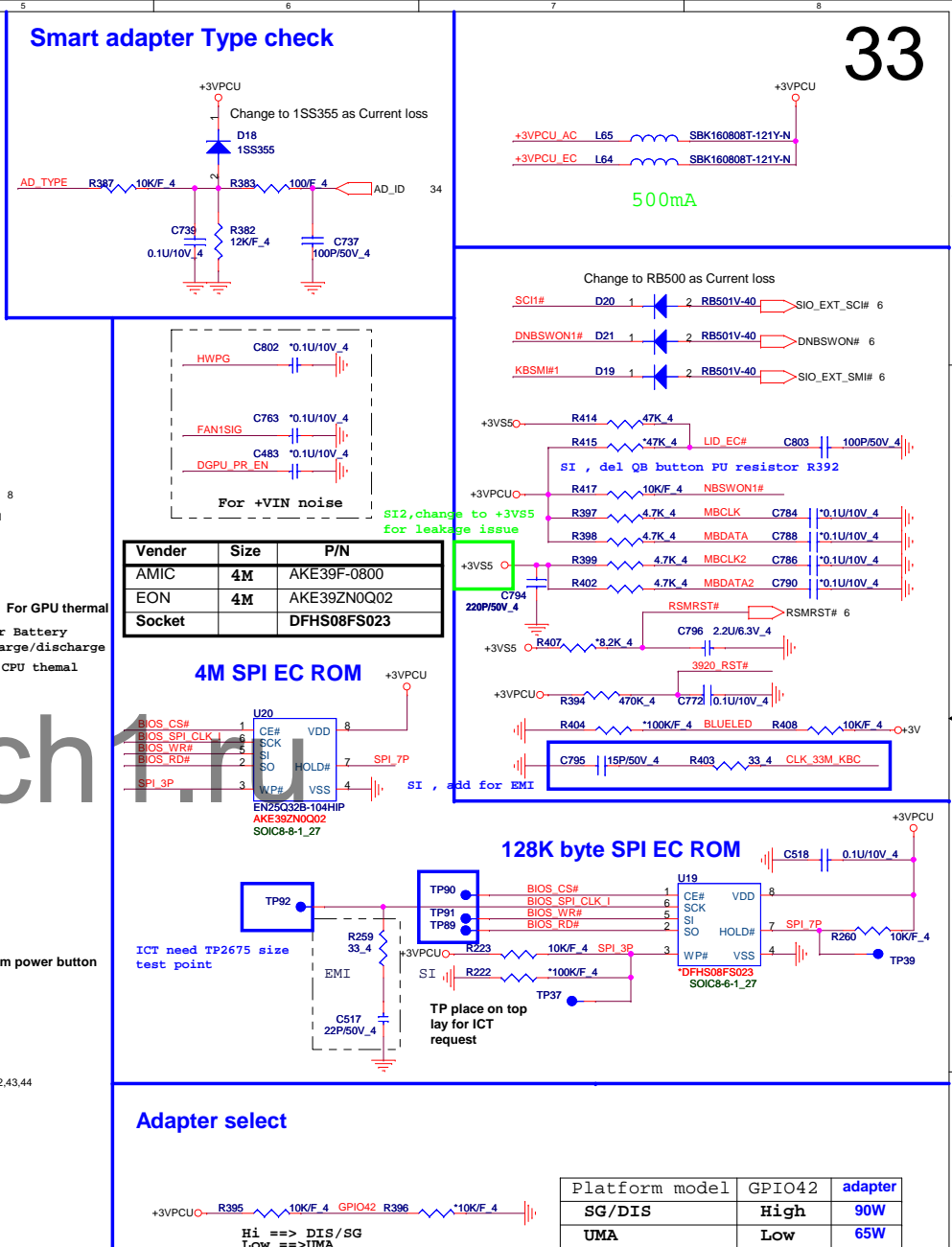
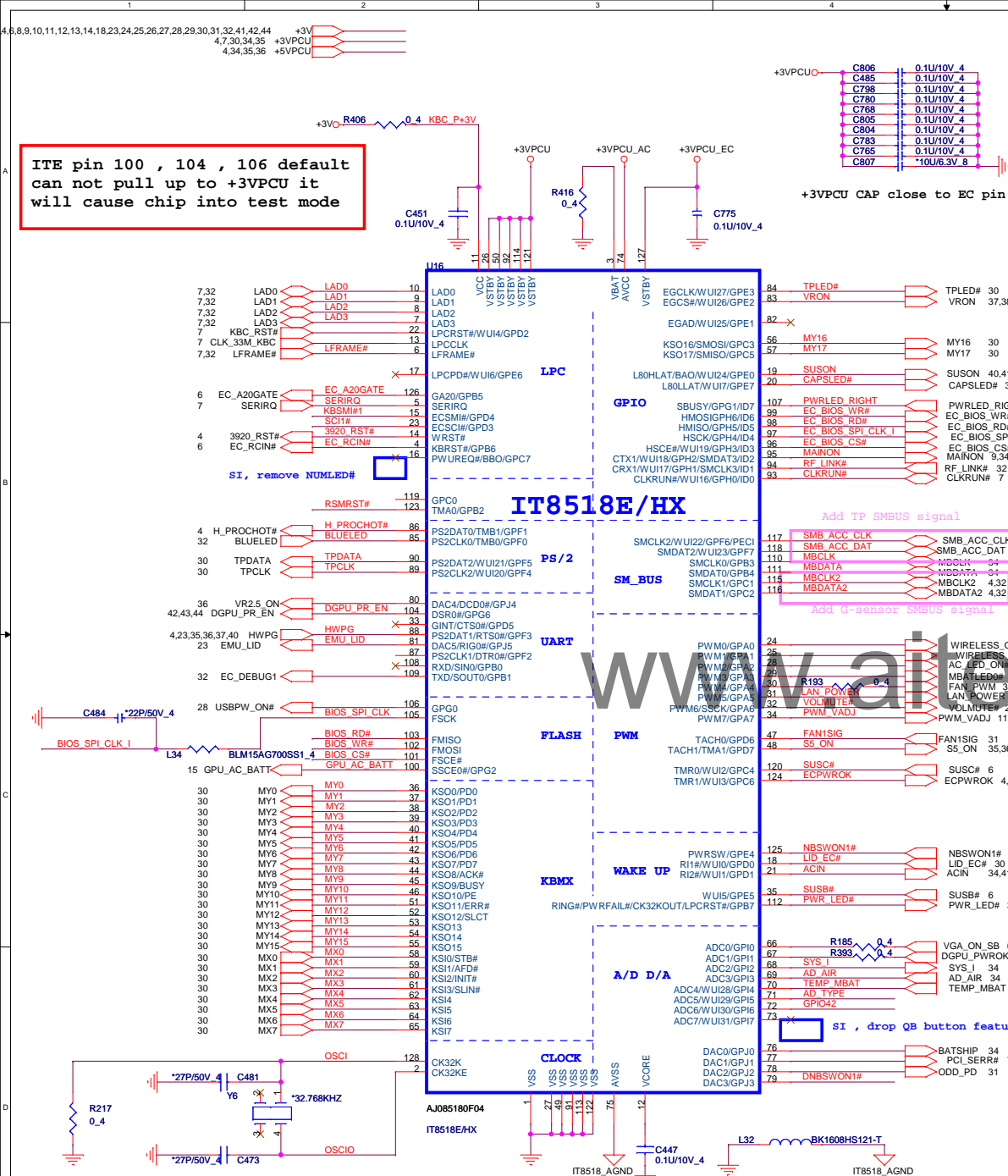


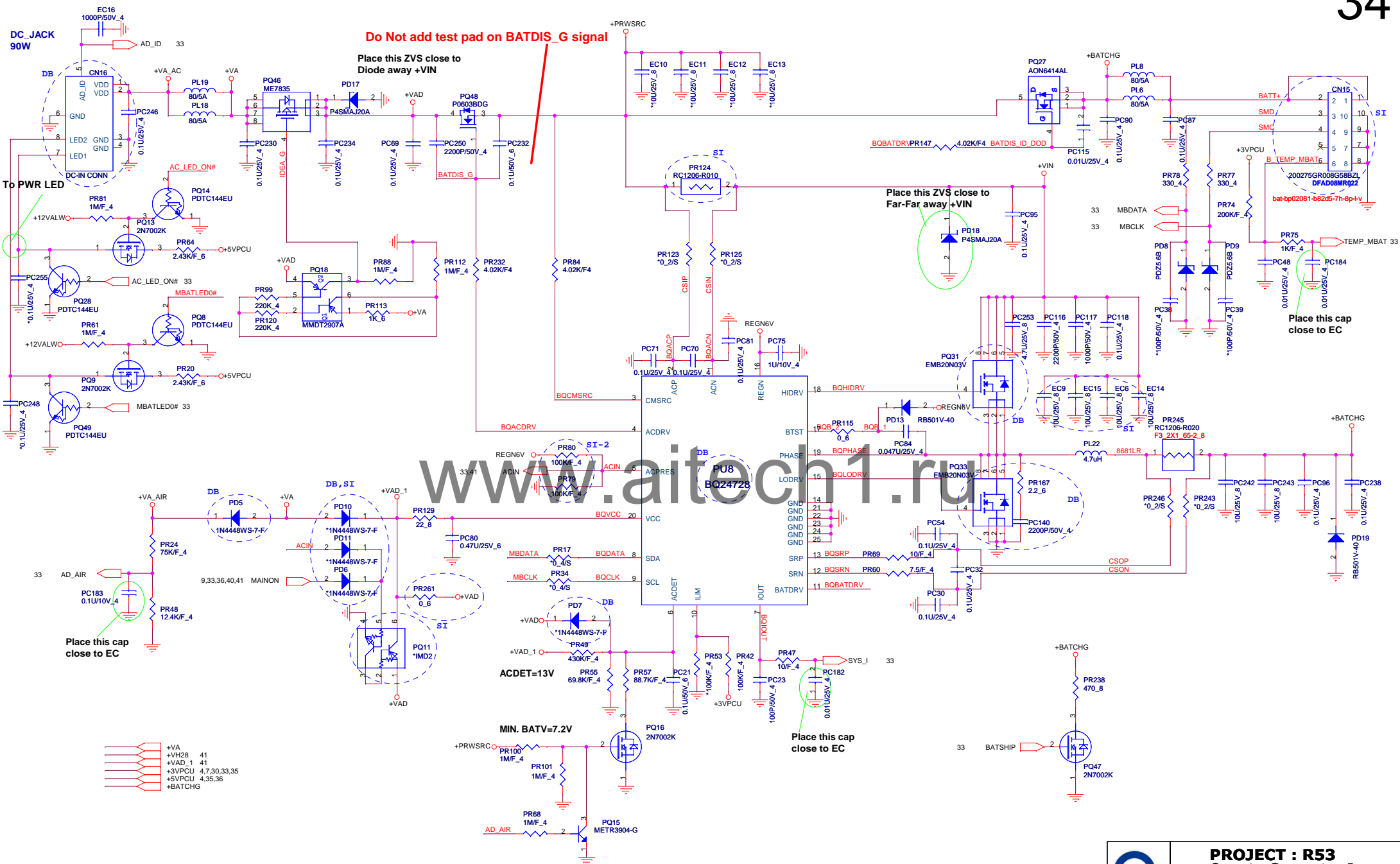




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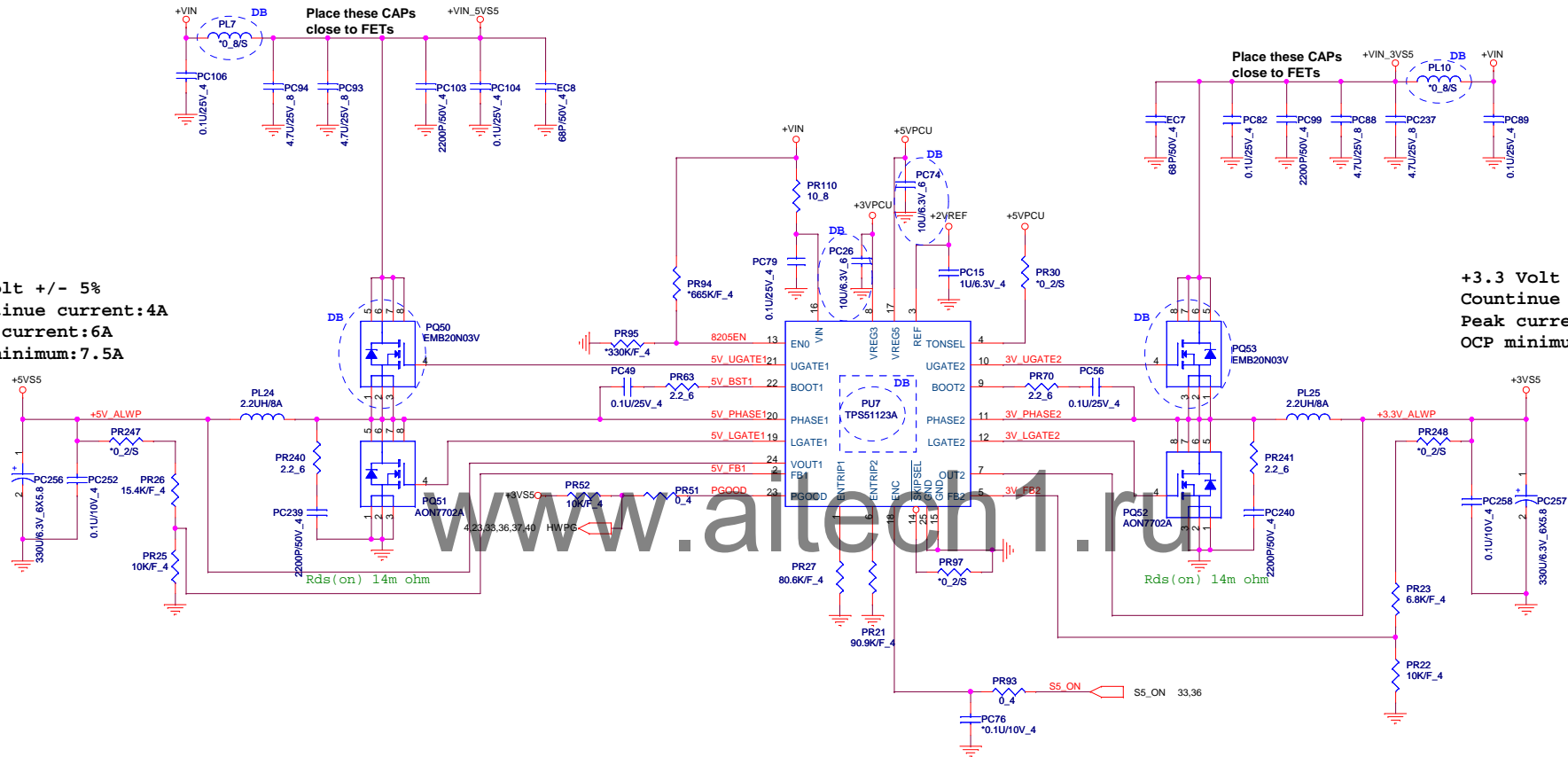




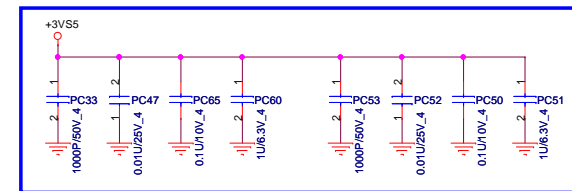


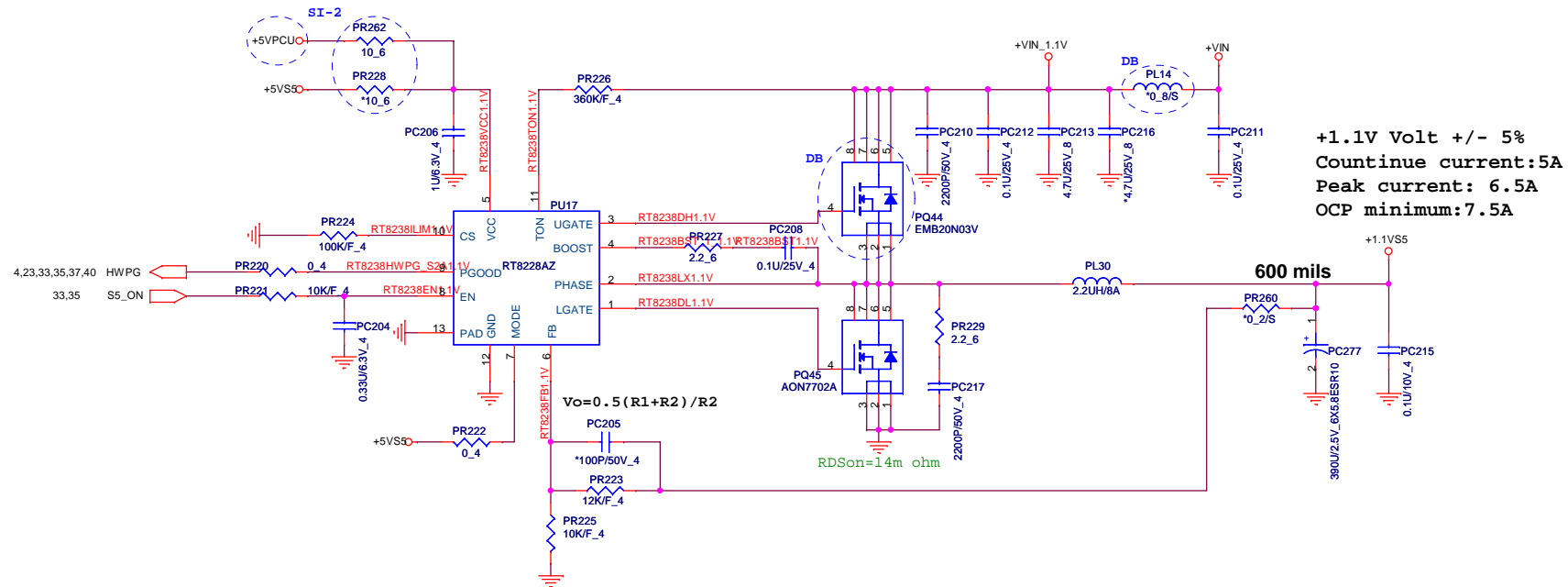
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

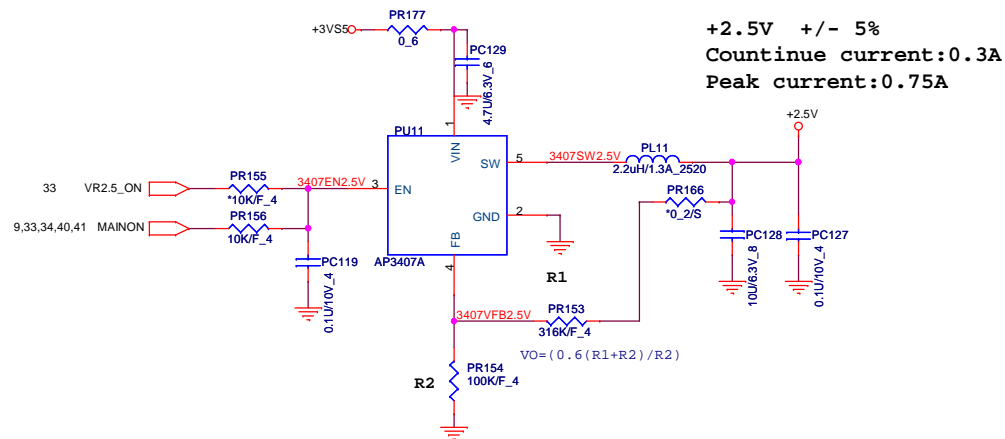


DB for prevent interference



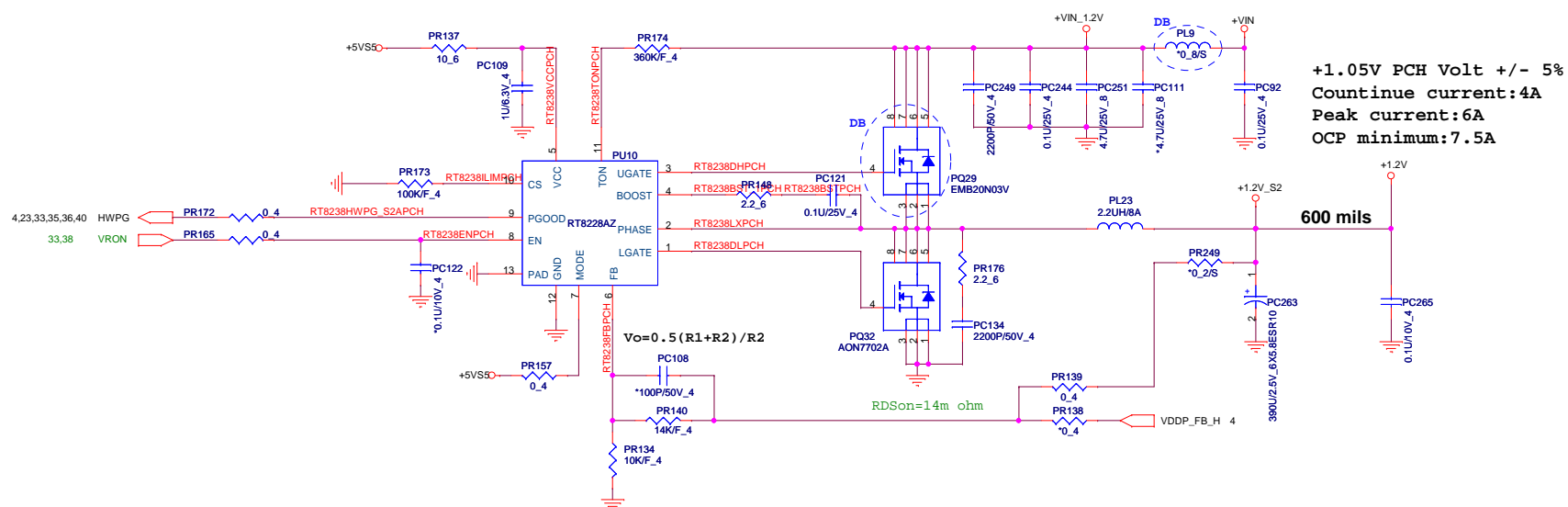


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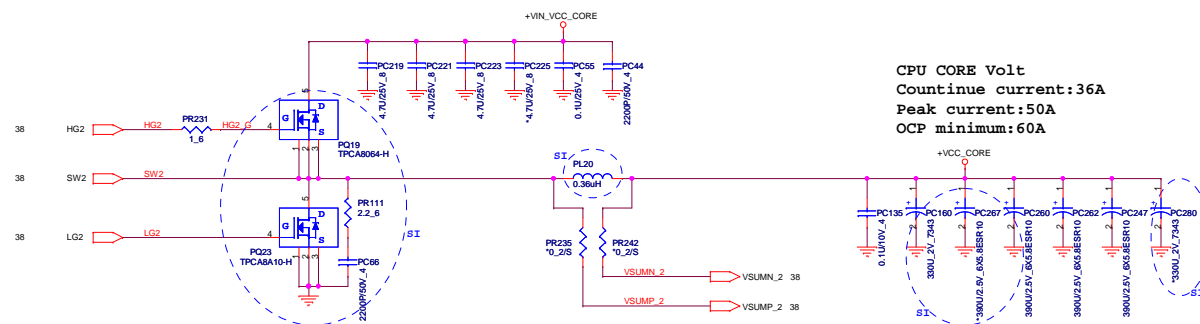
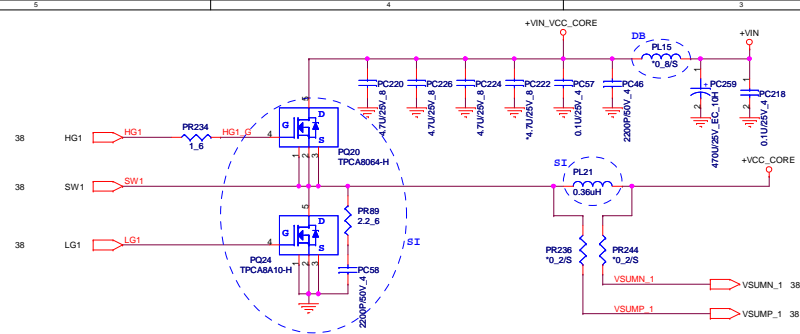


PROJECT : R53
Quanta Computer Inc.

| Size | Document Number | Rev |
|---------------------------------|-----------------------|-------|
| Custom | +1.1VS5 (RT8228)/2.5V | 1A |
| Date: Friday, November 11, 2011 | Sheet 36 | of 44 |

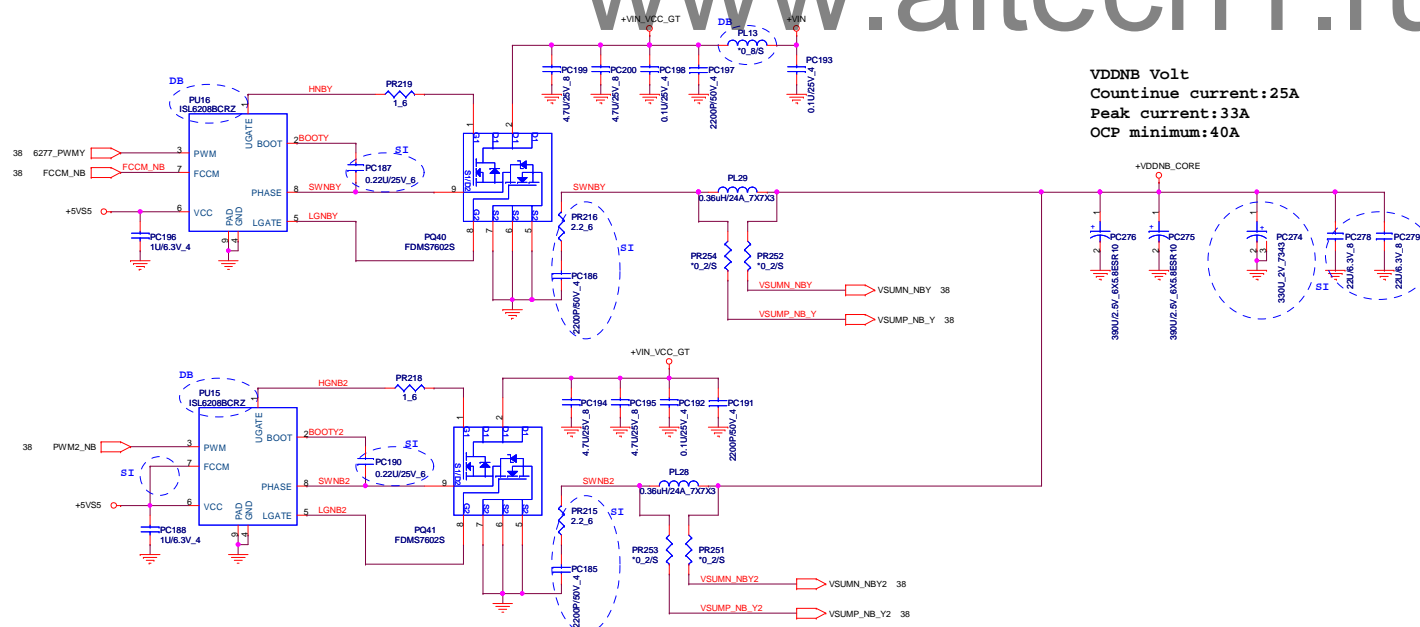


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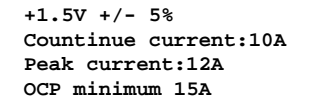


```
CPU CORE Volt
Continue current:36A
Peak current:50A
OCP minimum:60A
```

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VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A

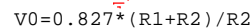


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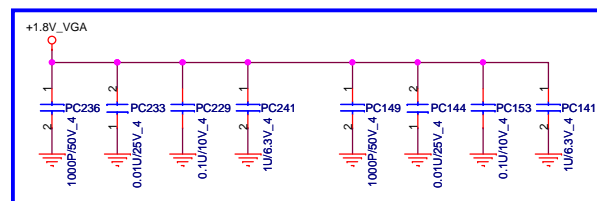


| Symour-XT | PWRCNTL2 (GPIO16) | PWRCNTL1 (GPIO20) | PWRCNTL0 (GPIO15) | V-CORE |
|-----------|----------------------|----------------------|----------------------|--------|
| L | 0 | 0 | 0 | 1.0V |
| M | 0 | 0 | 1 | 0.9V |
| H | 0 | 1 | 0 | 0.875V |
| | 0 | 1 | 1 | 0.85V |
| | 1 | 0 | 0 | 0.8V |
| | 1 | 0 | 1 | 0.75V |



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DB for prevent interference

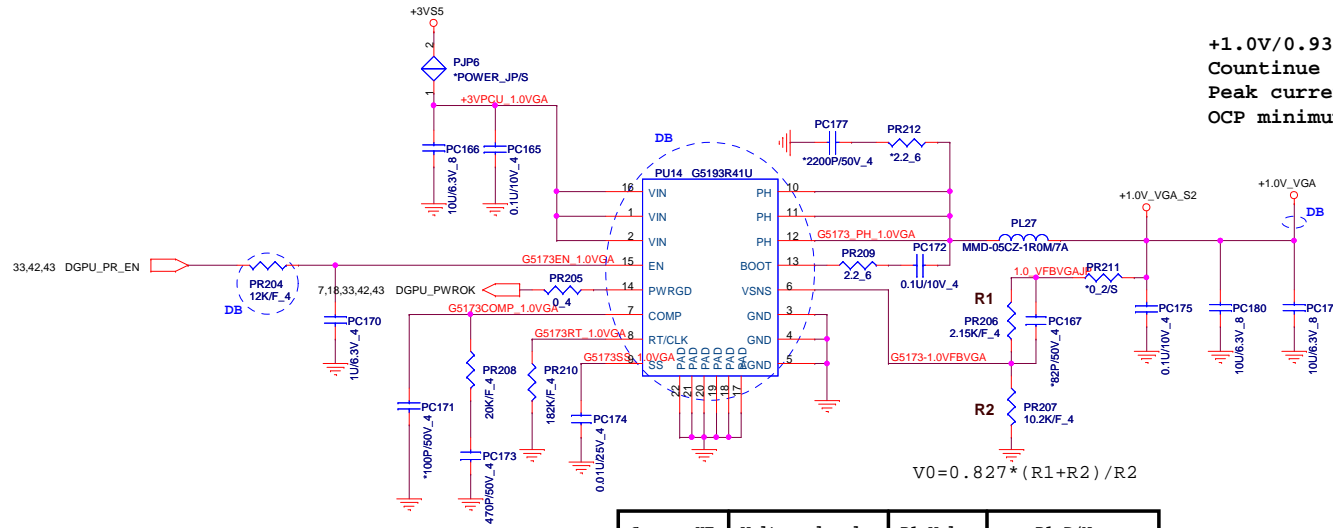


PROJECT : R53
Quanta Computer Inc.

| | | |
|---------------------------------|--------------------------------------|-----------|
| Size Custom | Document Number +1.8V_VGA (G5193) | Rev 1A |
| Date: Friday, November 11, 2011 | Sheet 43 of 44 | |

+1.0V/0.935V +/- 5%
Continue current:2A
Peak current:3A
OCp minimum 4.5A

| | |
|-----------|--|
| +3V | 2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42 |
| +VIN | 23,34,35,36,37,39,40,41,42 |
| +3VS5 | 3,4,6,8,9,10,12,33,35,36,41,42 |
| +5VS5 | 27,28,30,35,36,37,38,39,40,41,42,43 |
| +3V_VGA | 18,30 |
| +12VALW | 9,34,41 |
| +1.5VSUS | 2,3,4,5,12,13,40,41 |
| +1.5V_VGA | 18,20,21,22 |



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